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VOICE OF THE ENGINEER

JUNE **24**
Issue 12/2010
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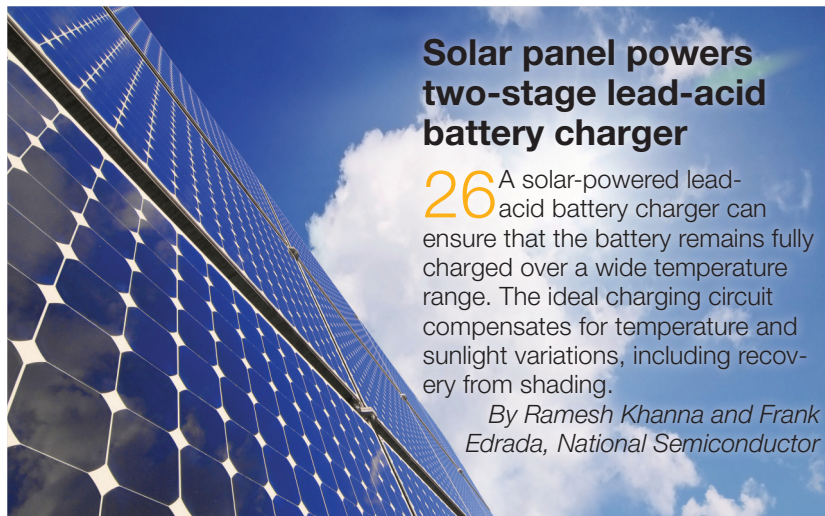


Testing embedded data buses and analog signals

36 Instrument makers help designers measure the bewildering array of analog and digital signals embedded processors, FPGAs, and application-specific custom and standard ICs can generate.

By Rick Nelson, Editor-in-Chief

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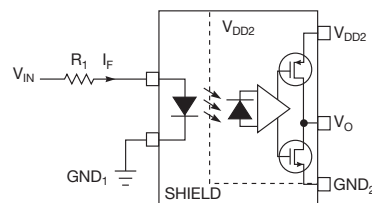
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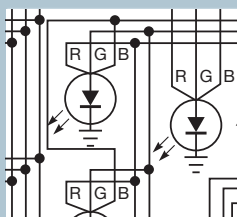


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Eco-Friendly Technologies with Ceramics

Samsung's **Passive Components** promoting low-carbon green growth



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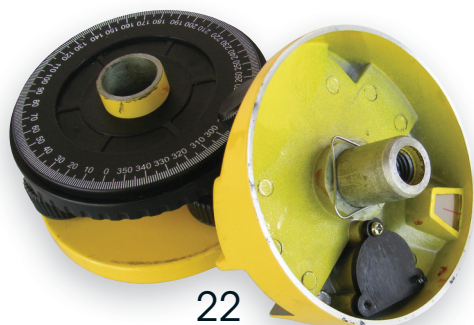


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ONLINE ONLY

Check out this Web-exclusive article:

Programmability to prepare for the edgy access

Intense competition and the need for more capacity push broadband service providers to deploy fiber and new carrier-Ethernet technologies farther out in the network. The access becomes more intelligent and therefore more important for vendors and service providers alike.

→www.edn.com/100624toca

Designing with LEDs

Practical, inexpensive HB LEDs (high-brightness light-emitting diodes) are here. Now, what can we do with them, and what will be their impact on electronics and customers? Read more online.

→www.edn.com/leds

PRACTICAL CHIP DESIGN

How do we somehow herd architecture, IP, design, and verification into a successful tape-out? In this blog, *EDN* Executive



Editor Ron Wilson explores how IC-design teams really work: the struggle for power efficiency and performance, wrestling with semiconductor processes and design methodologies, and the challenges of global design teams.

Sample a few recent blog entries at the links below:

Device-level extraction becomes an issue for SOC designers

→www.edn.com/100624tocb

Blowouts, elementary school, and the future of democracy

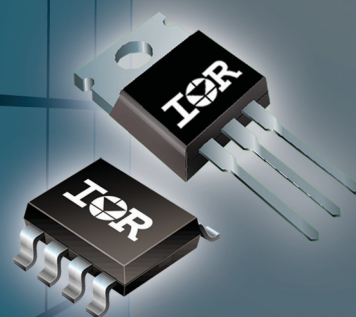
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V _{FE} (V)	<-200			
Sw Freq. max (kHz)	500			
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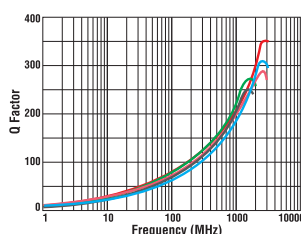
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29

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These tiny new air core inductors have the highest Q and current handling in the smallest footprint.

Coilcraft's new SQ air core inductors have unmatched Q factors: most are above 200 in the 1-2 GHz range! That's 3 times higher than comparably sized 0805 chip coils.

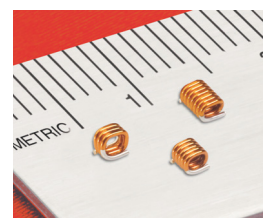


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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Putting hot on the spot

On a recent trip to South Korea, I brought both my Apple MacBook Air and my iPad. I stayed at a nice hotel in Seoul that came with complimentary Wi-Fi service. As I soon discovered, though, the service was restricted to a single device—that is, one MAC (media-access controller) per room. After wirelessly connecting the iPad, I attempted to register the MacBook Air using the same last-name/room-number combination, which the system summarily rejected. A call to the front desk got me going again with my primary computer, but I decided not to push my dual-computer luck.

The experience reminded me of the concept of a personal hot spot that enables multiple devices to link with the same WAN (wide-area-network) connection and each other at no incremental charge over a single-device case. My room also offered a Category 5 Ethernet cable, for example. If I had remembered to pack my small-form-factor travel router, I could have employed it to achieve my shared-access objective.

If the hotel hadn't offered Category 5, however, I couldn't have used the travel router even if I'd brought it with me on the trip. The 54-Mbps 3Com OfficeConnect Wireless 11g travel router supports router, access-point, and client modes, but it doesn't offer a wireless-to-wireless bridge option. Even if it did, such a non-standard mode is rarely usable in practice, plus it would have required knowledge of the hotel router's MAC address. And, because bridge mode simply passes along client MAC addresses to the hotel router rather than acting as a router itself, I'd still get charged for per-client access.

Another option would have been to employ a cellular router. This approach would have required a USB (Universal Serial Bus), PCMCIA (Personal Computer Memory Card Industry Association), or ExpressCard cellular adapter or a supported USB-tethered mobile phone and an associated cellular-service plan. Verizon recently took cellular simplicity to the next level with the Novatel Wireless-developed mobile Mi-Fi, which both embeds the cellular subsystem and operates with an integrated long-life battery. Sprint predictably followed in its CDMA (code-division/multiple-access) competitor's path, as have other cellular providers. More recently, Sprint upped the ante with the Overdrive, a portable hot spot that supports both EVDO (evolution-data-optimized) and newer, faster WiMax (worldwide-interoperability-for-mobile-access) technology.

What happens, though, if you lack the fiscal resources or, for that matter, the desire to tote multiple gadgets for an additional cellular-data-supportive rout-

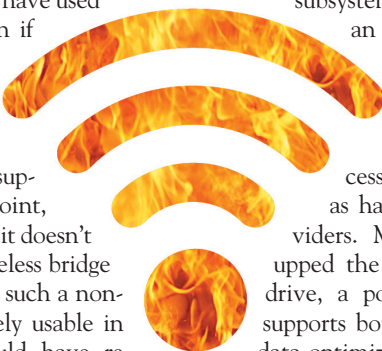
er along with you on future trips? What if your handset or service plan doesn't support USB or Bluetooth phone-as-modem tethering? Devices such as the iPad "conveniently" support neither the DUN (dial-up-networking) nor the PAN (personal-area-networking) Bluetooth profiles. Therefore, they don't allow you to wirelessly piggyback on your phone's cellular-data features. In exchange, you must pay for a separate cellular plan for the tablet.

In such cases, you could instead tap into your phone's built-in Wi-Fi subsystem, transforming it into a configuration that primarily transmits rather than receives. MyWi for the iPhone, for example, purports to transfer data between the handset's integrated cellular and Wi-Fi links for subsequent handshaking with 802.11-connected clients. Similar software packages for other mobile operating systems are also available. Palm's webOS, Version 2.2 of Google's Android OS, and the Android 2.1-based Sprint/HTC Evo 4G (fourth generation) come with hot-spot features.

Perhaps you'd prefer to dispense with slow, glitchy cellular connectivity and leverage the built-in Ethernet capabilities of your laptop. Both OS X and Windows support spanning between a wired-Ethernet connection and Wi-Fi—an approach that can transform your computer into a wireless hot spot so that other LAN clients can connect to it. It's no problem if you lack an available Category 5 connection. Intel's latest drivers enable Windows 7's built-in virtual-Wi-Fi feature by creating a virtual wireless adapter. And third-party software completes the Windows 7 picture for other companies' wireless adapters. Keep in mind that, before the emergence of Windows 7 Virtual Wi-Fi and Connectify, the implemented function was that of an access point, not a router, so the approach doesn't support sharing a common hotel-router connection among LAN clients.

Who says tech innovation is over? **EDN**

Contact me at brian.dipert@cancom.com.



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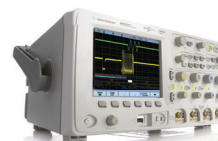
100 MHz - 500 MHz



100 MHz - 1 GHz



60 MHz - 200 MHz



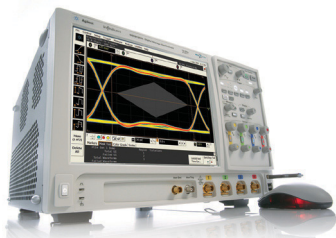
100 MHz - 1 GHz



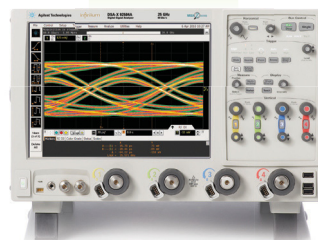
DC - 90 GHz Sampling



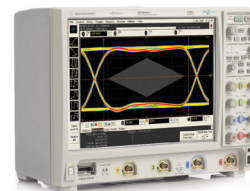
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Tiny PSIP delivers 113W/in.²

Enpirion has introduced a family of ultrasmall PSIP (power-supply-in-package) devices. The EN6300 series of voltage-mode, synchronous, buck dc/dc converters includes the 3A EN6337QI and the 4A EN6347QI, both measuring 4×7×1.85 mm in 38-pin QFN packages; the 8A EN6360QI, measuring 8×11×3 mm in 68-pin QFN packages; and the 12A EN63A0QI, measuring 10×11×3 mm in 76-pin QFN packages. The nonisolated devices achieve 113W/in.² power density, or 17.6W/cm², by integrating the inductor, power switches, gate drive, controller, and loop compensation.

Input voltage ranges from 2.375 to 6.6V, and peak efficiencies for the parts are 95 and 96% for the 6337/47 and 6360/63A0, respectively. Enpirion claims that the efficiency curve flattens across the load range rather than peaking sharply at full load.

The parts target use in applications including blade servers, RAID (redundant-array-of-inexpensive-disk) storage systems, LAN/

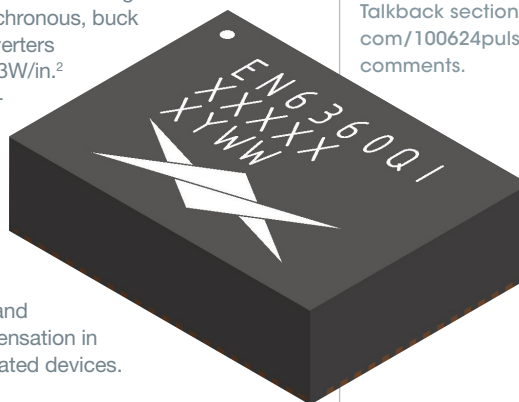
SAN (local-area-network/storage-area-network) adapter cards, wireless base stations, industrial automation, test and measurement, embedded computing, communications, and multifunction printers. Prices are \$2.71 (1000) for the EN6337, \$3.43 for the EN6347, \$6.64 for the EN6360, and \$10 for the EN63A0.

—by Margery Conner

►Enpirion, www.enpirion.com.

The EN6300 series voltage-mode, synchronous, buck dc/dc converters achieve 113W/in.²

power density by integrating the inductor, power switches, gate drive, controller, and loop compensation in the nonisolated devices.



TALKBACK

"Many ... want all jobs, except theirs, modified to the point that they can be done by any addle-brained slacker with a cell phone in his or her ear."

—Engineer and technical writer William Ketel, in *EDN's* Talkback section, at www.edn.com/100624pulsea. Add your comments.

Smart-grid chips integrate functions as meter vendors aim for standards

Freescale has fleshed out its smart-power-meter-IC family with its announcement of the MC9S08GW64 chip, which integrates gas- and water-metering functions. The company based the chip on an 8-bit S08 core. It includes an electricity-metering analog front end with two independent 16-bit SAR (successive-approximation-register) ADCs and a programmable delay block for phase-error compensation. The device joins Freescale's line of smart-meter chips, including the MCF51EM256, which uses a 32-bit Coldfire V1 microcontroller core for single- and three-phase electricity meters, and the MC9S08LH64, which also uses the S08 core, for low-cost, single-phase electricity meters.

Freescale goes beyond the usual reference design to provide complete multiple designs, including CAD drawings for the plastic

enclosure. Customers can leave all of the design to Freescale and customize only the meter's software.

Freescale is not alone in the push to integrate as much capability as possible into its metering chips. Accent (www.accent-soc.com) announced in early May an SOC (system-on-chip) platform for smart-metering designs. The company claims that the product allows customers to receive a customized version of a smart-meter SOC with a turnaround time of months rather than more than a year for a conventional custom SOC. Analog Devices (www.analog.com), Teridian (www.teridian.com), and Texas Instruments (www.ti.com) also offer highly integrated smart-meter chips.

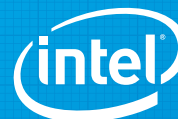
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Isolated POL converter combines best of two power-bus architectures

Today's datacom- and telecom-server systems commonly use either the DBA (distributed-bus architecture) or the IBA (intermediate-bus architecture). The DBA backplane bus performs an ac-to-dc conversion—typically of 48V—with multiple lower-voltage, isolated POL (point-of-load) dc/dc converters. These isolated POL converters are efficient but require some extra board space and expense due to their isolating transformers.

An IBA approach has one isolating dc/dc converter that feeds into multiple lower-voltage nonisolated POL converters. By having just one isolating power-conversion stage, you gain space and eliminate the cost of the additional isolating transformers. One drawback of the IBA approach is that it has a lower overall system efficiency because of the double conversion that the intermediate isolated stage and the nonisolated converters require. In addition, this approach usually has higher distribution losses as power moves at lower voltages and thus higher currents with their attendant resistive losses.

In recent years, server-power subsystems have placed a premium on lower price and smaller footprint, driving the popularity of IBA systems. Rising energy prices and power-supply real-estate costs are dictating a need for efficient, space-saving

surface-mount PSIP (power-system-in-package) platform measuring $0.87 \times 0.65 \times 0.27$ in. for applications in which board space, airflow, and height dimensions are critical.

The PI3101 operates over an input-voltage range of 36 to 75V dc and provides a regulated 3.3V output at an output current as high as 18A. The PI3101 can withstand input-voltage transients as large as 100V for 100 msec and provides 2250V input-to-output isolation.

The Cool-Power platform uses the company's PSIP to achieve a switching frequency of 900 kHz, allowing for the use of passive components. The chip achieves as much as 87% efficiency with a power density of 400W/in.³. The chip has no digital-communications capability, relying on traditional analog-programmable features, including $\pm 10\%$ output-voltage trimming, programmable soft-start capability, remote on/off enable, and an accurate temperature-monitor function that provides an analog output voltage proportional to the internal temperature of the product. This monitor also serves as a fault alarm. The device sells for \$29.97 (1000).

—by Margery Conner

► **Picor**, www.picor.com.



Picor's Cool-Power platform of low-power dc/dc converters achieves high-efficiency power conversion in minimal space.

power subsystems, however.

To address these needs, Picor's new Cool-Power platform of low-power dc/dc converters combines attributes of both DBA and IBA to achieve a high-efficiency power-conversion system in minimal space. The first member of the family, the PI3101, combines isolation, voltage transformation, and output regulation in a high-density,

PLATFORM MANAGES COMPUTING CLOUD

Wireless-sensor networks require a lot of data manipulation, which in turn implies a computing "cloud"—the use of large numbers of computers, often over distributed data centers, to seamlessly process and store large amounts of data.

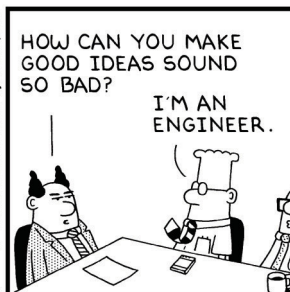
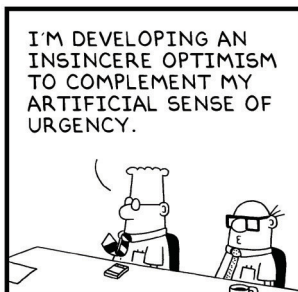
Small and midsize companies that want to delve into the wireless-sensor-network market may not decide to develop the software-support system for cloud computing because their expertise lies elsewhere. To fulfill these companies' needs, Digi International recently announced the iDigi platform for machine-to-machine network management, enabling secure remote access, control, and management of network-connected devices and cloud-based application development.

The iDigi platform allows manufacturers to remotely configure, upgrade, and diagnose problems with their products and monitor performance monitoring. This approach reduces repair costs and allows OEMs to deliver products with active supply replenishment, remote-configuration services, and downloadable features. Device configuration and maintenance require no travel. Prices start at \$1.99 per device per month; volume discounts are available.

—by Margery Conner

► **Digi International**, www.digi.com.

Dilbert By Scott Adams



Rarely Asked Questions

Strange stories from the call logs of Analog Devices

How to Avoid Burning Cakes

If only King Alfred had had better oven temperature measurement he need not have allowed the peasant woman's cakes to burn. And even in 880 A.D. it would have been possible to make a thermocouple had he known how.

Q. In an earlier RAQ you said that silicon ICs could be guaranteed between -55°C and $+155^{\circ}\text{C}$ but might work (without guarantees) over a somewhat wider range. How does one measure temperature outside the silicon range?

A. Thermocouples are very simple devices which can measure temperature over a very wide range.

If we have two conductors of different material joined at two points which are at different temperatures, there will be an emf (electromotive force) in the loop so formed—this emf is a function¹ of the temperature difference and can be used to measure temperatures as high as 2300°C and as low as a few Kelvin. One junction is at the temperature to be measured and the other (often known as the “cold” junction, even if it is at a higher temperature than the one being measured) is at a reference temperature (in the past a mixture of ice and water was often used to provide a 0°C reference).

Two pieces of wire of different materials are simple and, usually, inexpensive², so thermocouples are widely used. Where the reference will normally be within $\pm 10^{\circ}\text{C}$ of room temperature and accurate measurement is unnecessary, it is quite usual to use an uncompensated thermocouple for measurements. An example is the flame sensor in a boiler.



If reasonable accuracy is required, the cold junction must be held at a known reference temperature—which is inconvenient, as ice may be unavailable. But the cold junction need not be at a constant temperature as long as it is always known. The cold junction temperature, which is unlikely to be outside -55°C to $+155^{\circ}\text{C}$, may be measured with a silicon sensor; we then use the emf and the cold junction temperature to calculate the “hot” junction temperature.

This “cold junction compensation” may be done by a digital controller, but it is quite possible to integrate the cold junction sensor, the thermocouple amplifier, and the compensation in a simple analog chip. The AD594/AD595 and AD8494/AD8495/AD8496/AD8497 are examples of such circuits; if King Alfred had had one the cakes would have been perfect.

¹The function is (approximately) a polynomial of 5th – 13th order, but for some thermocouples simple proportionality is adequate over some ranges.

²Platinum (B, R & S) and chromel/gold-iron thermocouples are among the expensive exceptions to this.



Contributing Writer
James Bryant, ADI's European Applications Manager from 1982 through 2009, continues to find interesting projects within Analog Devices. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

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Signal-generator family reaches 70 GHz with low phase noise

At the IMS (International Microwave Symposium, www.ims2010.org), which took place in May in Anaheim, CA, Anritsu introduced the MG3690C series of RF/microwave-signal generators. The generators allow engineers to conduct accurate tests on subsystems, especially those in local-oscillator-substitution and clock-generation applications, according to Bob Buxton, marketing manager in the general-purpose-business unit of Anritsu's microwave-measurement division. The MG3690C instruments can test microwave components, subsystems, and systems during design. Their 5-msec switching lets the units maximize throughput in manufacturing applications.

In addition, they can perform signal simulation to test and verify radar and communications systems.

The MG3690C, the latest member of the company's synthesizer family, generates signals from 0.1 Hz to 70 GHz. Instruments in the family can produce baseband, IF, RF, and microwave signals to maximize equipment use and reduce cost of test.

Options enable phase-noise performance of 2115 dB/Hz at 20 GHz at a 10-kHz offset. This phase-noise performance ensures the simulation of devices under test with known-good signals, thus enhancing the integrity of the measurement and reducing the time it takes to track down test-equipment-induced measurement problems. The instruments are

also suitable for digital datacom applications because their low phase noise minimizes instrument-induced clock jitter.

The MG3690C can generate pulses as narrow as 10 nsec to emulate a variety of signals. It can generate amplitude-leveled pulses as narrow as 100 nsec to minimize amplitude drift over time and temperature for tight test margins. Amplitude-leveled pulses also eliminate the need for a clockwise mode during

frequency changes and minimize the chances of damage to the device under test. The MG3690C series can generate doublet, triplet, and quadruplet pulses with independently set spacing and pulse width, making the signal generators well-suited to emulating a range of radar returns.

Models are available with top frequencies of 10, 20, 31.8, 40, 50, and 70 GHz. All models offer a 0.1-Hz starting-frequency option. The base price is \$17,800. —by Rick Nelson
▶ Anritsu, www.us.anritsu.com.



The MG3690C series of RF/microwave-signal generators allows engineers to conduct accurate tests on subsystems, especially those in local-oscillator-substitution and clock-generation applications.

PACKAGING GIVES HALF-BRIDGE MOSFET A 2% BOOST IN EFFICIENCY

Texas Instruments' NexFET-based CSD86350Q5D power block provides 2% better efficiency than—in half the area of—competitive power-MOSFET devices. TI optimized the device's packaging for low-voltage, high-current, high-frequency switching in half-bridge switching configurations for synchronous buck converters. The 1.5-MHz CSD86350Q5D comprises two asymmetrical NexFET power MOSFETs and owes its efficiency to an advanced packaging technology that targets low-voltage, synchronous, buck, half-bridge applications.

According to Jeff Sherman, power-stage-marketing engineer for TI, the two discrete NexFET devices have similar,

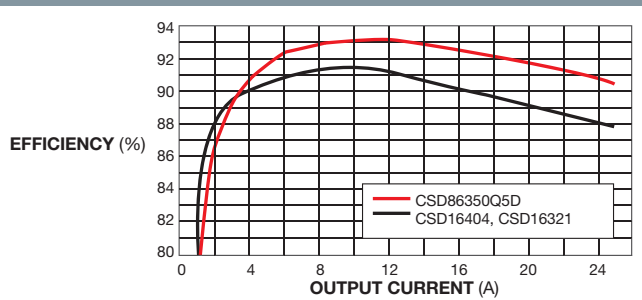
matched on-resistances. Most of the improvements in the newer devices come from the improved switching characteristics due to the reduced inductance between devices. TI vertically mounted the two FETs rather than laying them out side by side. Vertical mounting yields a shorter connection, resulting in lower parasitics and allows the use of copper

clips, resulting in the lower inductance than that of wire-bond leads. The lower inductance results in the 2% increase in efficiency, which translates to 20% less power loss.

The exposed ground pad on the package bottom mounts directly on the PCB (printed-circuit board) for a simpler board layout. MCMs (multi-chip modules) such as this one from

TI command premium pricing, but there is no premium for the package, says Sherman. Rather than use a second source, TI taps two supply chains to fabricate and assemble the device. The CSD86350Q5D sells for \$1.75 (1000).

—by Margery Conner
▶ Texas Instruments, www.ti.com.



The 1.5-MHz CSD86350Q5D comprises two asymmetrical NexFET power MOSFETs and owes its efficiency to an advanced packaging technology.

Medical Power Supplies...

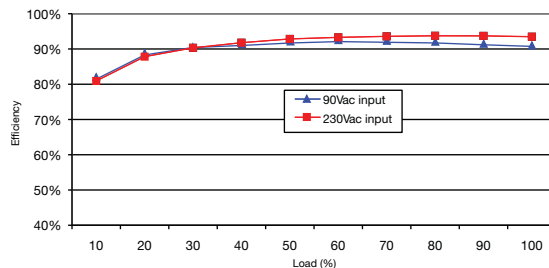


without the fan

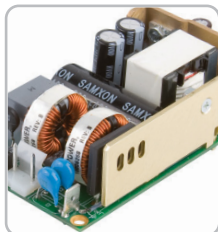


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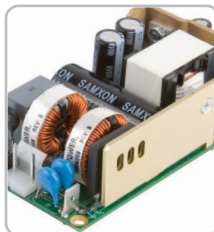
CCM250 - Award winning power supply



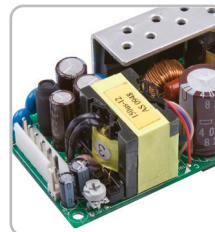
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VOICES

Moving to hire ground: Dice's Tom Silver on the improving tech-employment environment

There's certainly room for improvement, but the tech-employment environment has shown significant recovery so far this year. Tom Silver, senior vice president of North America at tech-focused online career hub Dice (www.Dice.com), in late May discussed the overall tech-employment market, employer confidence, and a recent Dice survey of 1200 tech professionals across North America regarding employee retention. Excerpts of that conversation follow. For more on the Dice retention survey, see www.edn.com/100624voices.

The May Dice Report estimated a little more than 69,000 open high-tech positions. Has hiring returned for high-tech and EE positions?

A We have 69,000 jobs on the site. That's up significantly from a year ago. It's up over 40%, which is great news. We think that's a pretty good indication that employer confidence is picking up, and we are seeing that as it relates to job counts.

In aggregate, the fact that employers are hiring suggests that their confidence in their business is improving. Certain positions, as they relate to technology, may have been put off for a while, and [employers] are now jumping back in. Projects are getting green-lighted, and we are seeing that evidenced by the fact that the job count is up.

Dice recently ran its first survey looking at employee retention. The responses showed that many tech employees intend to change

jobs in 2010 and could be persuaded to leave their current positions. Is talent poaching occurring?

A Not yet, but I think it will. The survey suggests not so much that poaching is happening, but it is really an indication of tech workers' willingness to jump. If you look at the data, 30% [of respondents] are saying they are getting more headhunter calls than they did at this time last year. That's an indication of the fact that activity is up. What's more interesting is that more than half of the people who responded say that they intend to move sometime in 2010. That's a scary number. Whether it's because of poaching, whether it's because of money, or whether it's for a change of scenery, overall, I think there is going to be a lot of turnover in the market.

Almost half of the survey respondents said that a 10% or less increase in



compensation would deter them from leaving a position. Was that surprising, given that employers cut many salaries by more than that during the downturn?

A It's surprising but not shocking. We run a salary survey every year. For the last several years, the expectation among tech workers was a 3 to 5% salary increase, and we saw the survey reflect that [increase]. This year, salaries were flat. To me, that [fact] suggests that people are coming to realize that salary increases are harder to find, that economic conditions are still pretty tough, and that 10%, for example, may not have had much traction in previous times, but today sounds pretty good.

Do you believe employers are aware of employee frustrations?

A Many employees would like to believe that, if they do a good job, they will be recognized, they will move ahead in their careers, and they will make more money. That doesn't always happen. As a matter of fact, that probably happens a lot less than anyone would like. But not everybody wants to complain about it for any one of a number of reasons. What you find is a growing frustration among employees, particularly tech pros, that they are doing this

great job and not being recognized. What makes it even worse is that, if you go back a year or so ago when the economy was tanking, tech-pro unemployment remained low compared to the overall average. Tech unemployment ranged about half of what overall employment was for all industries.

The tech market was tight. Companies were asking tech pros to do more and more with fewer and fewer people. Companies were not investing what they needed to in tech hires, and the frustrations among tech employees grew.

If half of the respondents said they planned to change positions in the year and the tech market is already tight, where is this new talent going to come from?

A That's a good question, but that's a question employers need to worry about. They may or may not be aware of growing dissatisfaction. [Employers need to] be aware of retention, be aware of the growing movement afoot [for employees] to perhaps show their dissatisfaction by leaving, and focus on some of the financial or nonfinancial things that are going to have an impact on employee satisfaction and retention.

Anything else on the survey or job market?

A We are happy ... that the job count is up 40% from where it was a year ago. ... The job count on Dice has been up over 100,000 at some points. The fact that there are [more than 69,000 jobs] out there today is better than it was, but we still think there is room to grow.

—interview conducted and edited by Suzanne Deffree

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BY BONNIE BAKER

Third round: Look at repeatability

System repeatability differs from system accuracy. With system repeatability, you compare the data from conversion to conversion. The specification that helps define repeatability is noise. For an analog device, such as a PGA (programmable-gain amplifier) or an ADC driving an amplifier, you take the noise-density performance at a frequency one decade less than the bandwidth of the device and multiply that value by the square root of the closed-loop bandwidth and $(\pi/2)$. The multiple of the square root of $(\pi/2)$ accounts for the noise in the region beyond the device's bandwidth. The equation for this calculation is available with the online version of this article at www.edn.com/100624bb.

When calculating the total noise in a system, you can use an rms (root-sum-square) formula to combine these noise sources at the input of the circuit. The equation for this calculation is also available at www.edn.com/100624bb.

If you allow only less than 0.5 bit of error, the PGA-SAR (successive-approximation-register) system can achieve 12-bit repeatability with an analog gain to 16V/V. The rms noise density at 10 kHz of the PGA116 and OPA350 in this circuit is 12 and 5 nV/ $\sqrt{\text{Hz}}$. The ADC's contribution to noise is 26.9 μV rms.

The PGA-SAR system cannot meet a 12-bit level of repeatability with PGA gains greater than 16V/V (Table 1). What about a delta-sigma system, however? When it comes to noise, the delta-sigma converter relieves the board designer from tedious analog calculations. For the ADS1258, the effective resolution is 19.5 bits. The translation of 19.5 bits of resolution into repeatable volts in a 5V system is equal to 12 μV rms of noise. Regardless of the process gain for the delta-sigma converter, the 12- μV -rms noise level applies to the convert-

er's performance across all gains (Figure 1, available with the online version of this article at www.edn.com/100624bb). This performance differs from that of the PGA-ADC circuit in which the PGA's gain affects the noise level.

If you look at the delta-sigma system from an input perspective, you can understand the size of the system's LSB (least-significant bit). When the process gain is one, the RTI (referred-to-input) system LSB size is 1.22 mV, with a noise level of 12 μV rms. As the process gain increases, the system's LSB decreases and the RTI noise remains constant. For instance, when the process gain is 128, the theoretical RTI LSB system is 9.54 mV, and the delta-sigma converter's noise level is still 12 μV rms. If you look at the delta-sigma converter in terms of noise in Table 1 (columns 6 and 7), you can see a good 12-bit system up to a process gain of 32.

The repeatability of the PGA-SAR system produces a 12-bit-ready system with analog gains of one to 16V/V. The repeatability of the delta-sigma system produces a 12-bit-ready approach with process gains of one to 32. In this evaluation, the delta-sigma system slightly surpasses the noise performance of the PGA-SAR system.

As you think about the speed, accuracy, and the repeatability performance of the PGA-SAR system and a delta-sigma converter, from the discussions in this column and my previous three columns (references 1 through 3), which system would you now select for your application circuit, or is there more to consider here? Send your thoughts to me at ti_bonniebaker@list.ti.com. **EDN**

TABLE 1 BASELINE DATA AND REPEATABILITY ERRORS

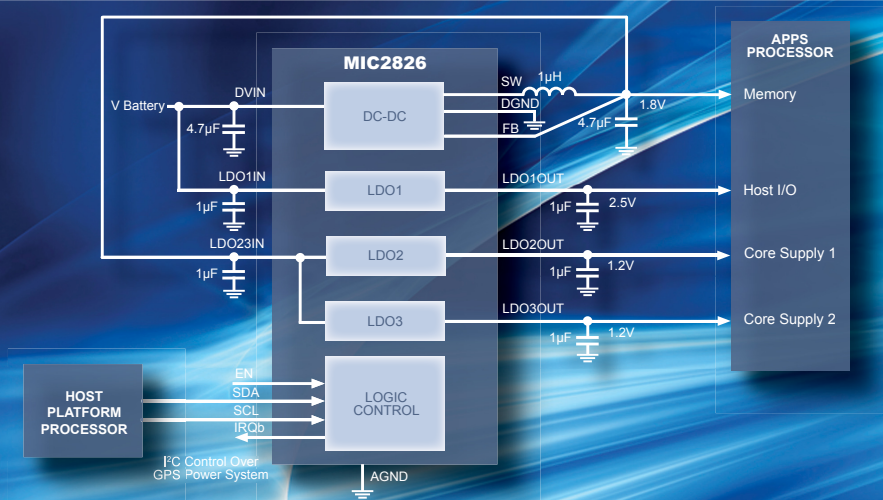
Analog or process gain	Baseline		PGA-SAR ADC		Delta-sigma ADC	
	System full-scale range (V, RTI)	System LSB size (μV , RTI)	Noise (μV , RTI)	Noise/system LSB	Noise (μV , RTI)	Noise/system LSB
One	5	1220.7	435.33	0.357	12	0.01
Two	2.5	610.35	218.34	0.358	12	0.02
Four	1.25	305.18	110.25	0.361	12	0.039
Eight	0.625	152.59	57.73	0.378	12	0.079
16	0.3125	76.29	33.07	0.433	12	0.157
32	0.1563	38.15	24.29	0.637	12	0.315
64	0.0781	19.07	13.47	0.706	12	0.629
128	0.0391	9.54	9.52	0.998	12	1.258

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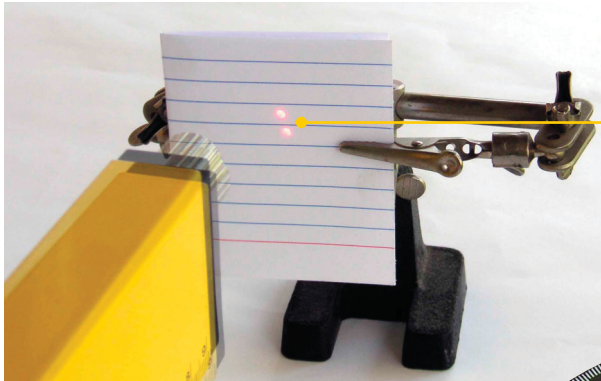
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The Titan 15000 laser level

Like any other engineer, I love tools. When I saw a laser-level kit selling for \$20 at a local electronics flea market, I purchased it with delight. My delight soon faded when I saw that the base was so wobbly that the laser spot would move up and down by more than 1° of arc. Prying into the interior of the base, it became obvious that the design had several shortcomings. After a failed attempt at a field expedient, I obtained a permanent fix with my belt sander. From now on, I will beware of bargain tools at the flea market.



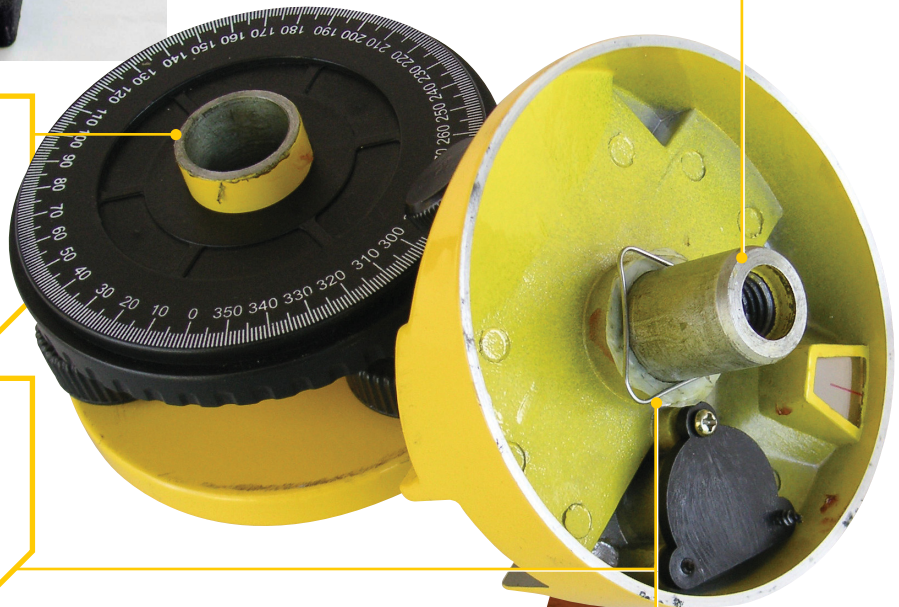
If you hold the base firmly against the table and put the slightest pressure on the laser, the spot would wobble due to the sloppy fit of the pivot mechanism.

A large plastic nut screws into this boss. Unfortunately, the boss is a bit long for manufacturing clearance, so the nut applied no pressure to the inner flange.

The pivot mechanism was poorly designed. The boss and sleeve had excessive clearance that allowed the base to wobble. The sleeve was too long, so the top rested on the inner boss flange rather than on the plastic outer rim of the base.

I took the level to a local burger joint as a team-building exercise. By cutting up a ketchup cup with a Swiss army knife and bending a paper clip, my fellow engineers fashioned a shim that considerably stiffened the assembly.

The fix involved sanding down the inner sleeve so that the top assembly would rest on its outer rim rather than the center post. Sanding the inner boss tightened the assembly. I sadly disposed of the paper clip and homemade shim.

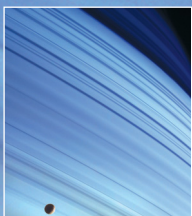


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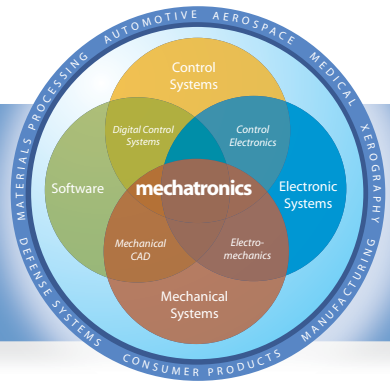


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Complexity demands a new engineering mindset

Engineering education is a great example of a complex system that must be transformed.

In mechatronic system design, we integrate. From the start of the design process, we combine the physical system with sensors, actuators, computer control, and human interfaces to give it some intelligence and decision-making capability.

At its heart, system complexity is synonymous with power. However, this power can be good or bad. If the complexity in any system is not tamed, the consequences can be devastating. We have witnessed some of the consequences of untamed complexity in the Chernobyl nuclear plant accident in 1986, the recent world financial meltdown, and now the Gulf of Mexico oil spill. All are examples of systems of unimaginable complexity—intended or not—that were left unmanaged without common-sense, human-centered checks and balances, which resulted in catastrophes of immense scope.

In a complex system, learning how all the pieces—constant and variable—interact gives a depth of understanding that averts catastrophe. That is what we mean by human-centered design—understanding the interfaces among technology, people, communities, governments, and nature. This is what makes complexity manageable.

All complex systems have, as a foundation, fundamental principles or core knowledge that we cannot ignore. However, there must also be a flexibility from the engineering perspective to respond to problems that inevitably arise. Clearly, the typical discipline-specific engineer is not well-equipped to manage such complexity; not even an engineer with multidisciplinary engineering breadth can do an effective job.

Complexity demands engineering skills with technology depth and also nontechnical breadth—specifically, human-centered design expertise that can manage complexity. This concept received wide acceptance at the IBM/IEEE Conference on Transforming Engineering Education, which took place April 6 through 9 in Dublin, Ireland. Jim Spohrer, director of IBM University Programs, saw it as essential to IBM's focus on service activities worldwide because every product has a service associated with it. The questions that arose at this conference were: "Why aren't we creating these engineers?" and "How do we ensure that they will be?"

The urgent problems society faces are multidisciplinary in nature, complex, and ever-changing. Engineering graduates need to be able to adapt and apply technology that is human-centered, desirable, feasible, viable, sustainable, usable, and manageable. Incoming students need to experience a culture change. They need to transform from the world of memorizing, test-taking, and focusing on grades, to the world of critical thinking and problem solving, turning easily accessible information into insight and understanding and taking responsibility for becoming an engineer.

So if we all know what should happen in engineering education, why is it not happening?

As I see it, there are two main impediments to engineering education reform. First, the silo structure in a typical engineering college does not foster reform. Engineering departments typically don't collaborate or interact in a multidisciplinary way and fail to realize that doing so would enhance, not diminish, what they do. Second, there is a failure of faculty members to leave their comfort zone, become involved in real-world problem solving, and respond to the challenges of teaching multidisciplinary engineering problem solving in a discovery-learning mode, rather than a lecture mode.

We need to unbundle and rebundle knowledge in engineering education to give it balance between theory and practice and relevance to the solution of the multidisciplinary problems society faces. Engineering education done in this manner can mitigate catastrophe. **EDN**

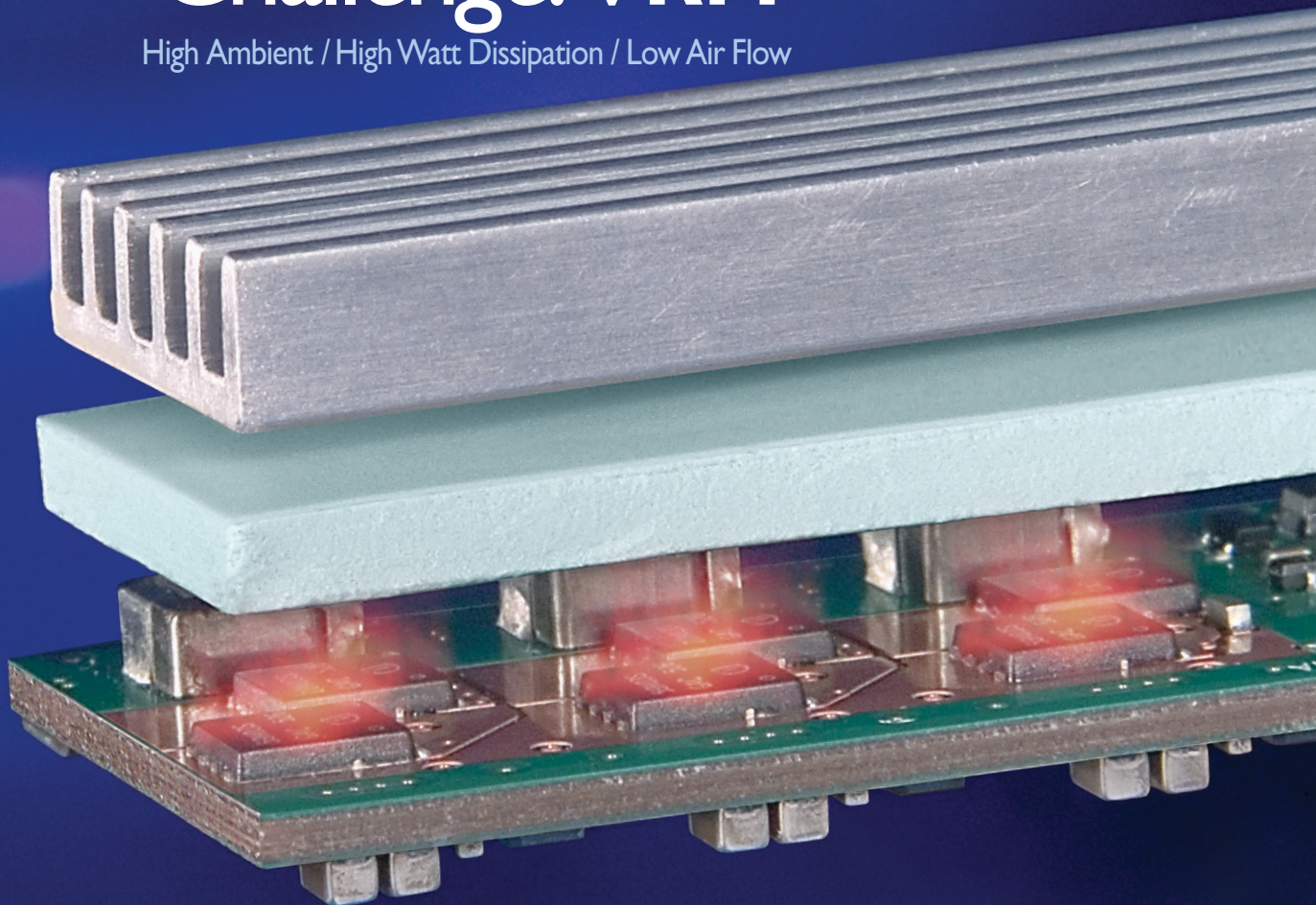


Kevin C. Craig, PhD, is the Robert C Greenheck chair in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University. For more mechatronic news, visit mechatronicszone.com.

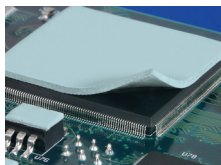
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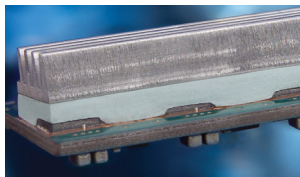
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Solar or photovoltaic panels comprise multiple solar cells that connect in series. An ideal solar cell appears as a current source that connects in parallel with a rectifying diode. The photovoltaic current, I_{PH} , depends on the sunlight falling on the solar cell. In the dark, a solar cell is simply a diode. A solar cell residing in shade has limited current-generating and -carrying capability, resulting in limited current-carrying ability for the entire solar panel.

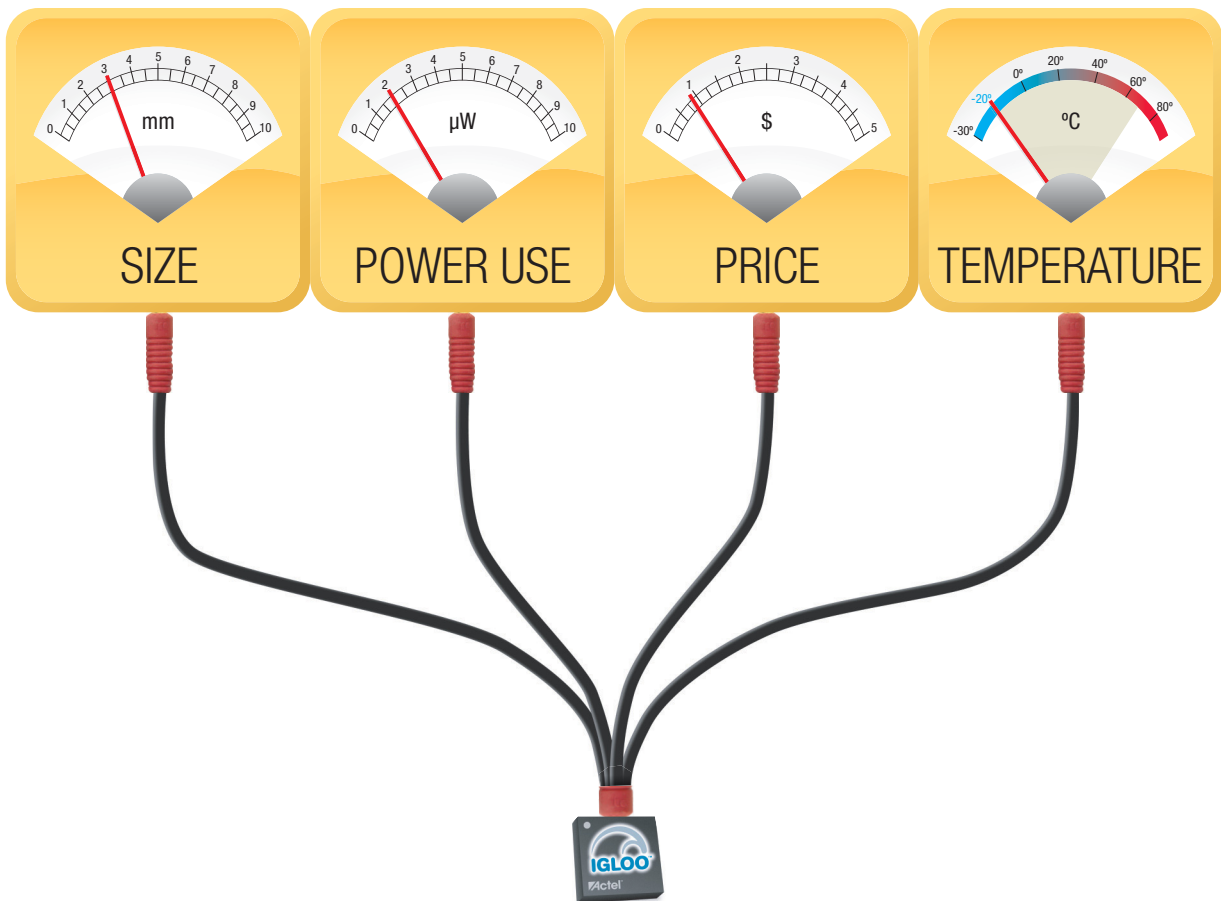
The current-output ability of a solar cell falls with a reduction in sunlight (**Figure 1**). **Figure 2** shows the effect of temperature on a solar cell's output voltage; that is, solar-cell output voltage decreases with an increase in temperature.

This design uses a solar panel comprising a series of solar cells to charge a lead-acid battery when the solar panel is operating at the maximum power point. A number of design steps are necessary to ensure that the cell operates continuously at the "knee" of the IV curve, thus providing maximum power to the load (**figures 1 and 2**).

The design in **Figure 3** uses an 18-cell, 3W SunWize Technologies (www.sunwize.com) SC3-6V solar panel as the input source. The design comprises one stage that monitors the solar-panel voltages using a SEPIC (single-ended-primary-inductor-converter) topology that employs a National Semiconductor (www.national.com) LM5001 controller. The LM5001 provides the output voltage that tracks the solar panel's output voltage over the temperature range. A simple, cost-effective thermal-monitor circuit using a string of BAT54 diodes tracks the solar panel's voltage over a temperature range of 25 to 100°C.

The second stage of the design takes the output of the first stage and boosts the input voltage to a nominal 13.3V at 25°C and 14.4V at 100°C. The second stage is configured as

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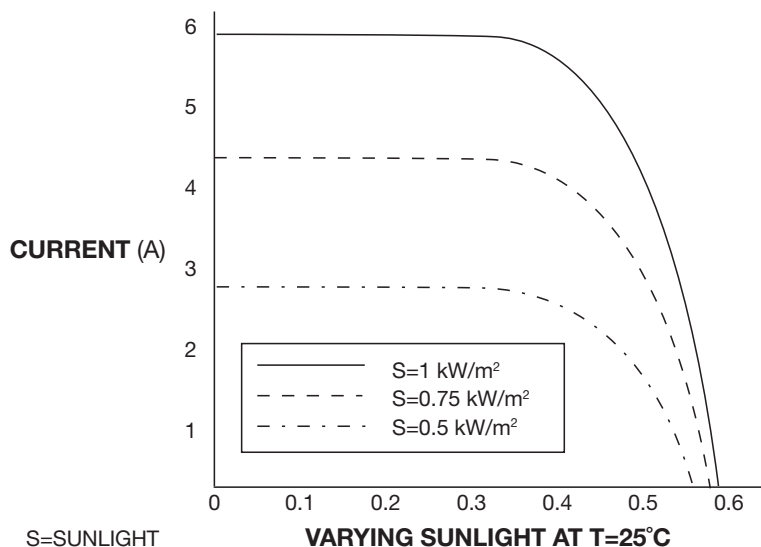


Figure 1 A solar cell's current output decreases with a reduction in sunlight.

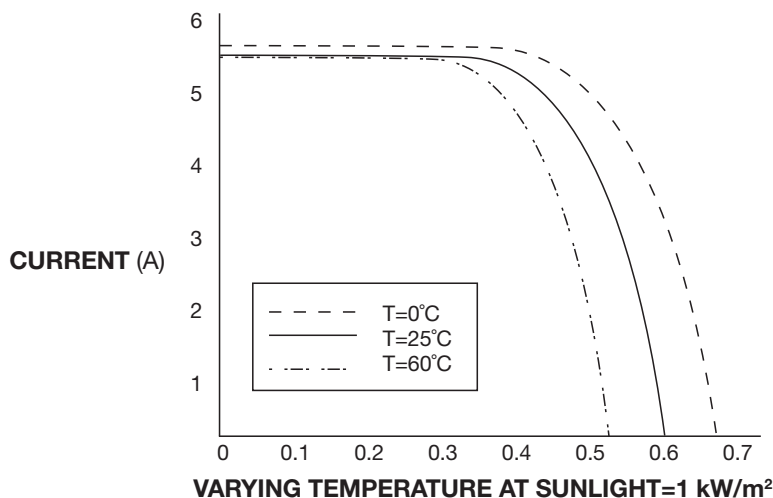


Figure 2 A solar cell's output voltage decreases with an increase in temperature.

AT A GLANCE

Although more advanced battery chemistries are available, lead acid is and will for some time be the predominant chemistry.

The charging circuit must be aware of and accommodate for solar-panel shading.

To maximize output power, the charging circuit must operate the solar panel at its maximum power point.

a constant-current controller to charge the 12V lead-acid battery that matches the optimum charge technique for a lead-acid battery. You can find detailed schematics for the two stages in the on-line version of this article at www.edn.com/100624df.

The charging current into the battery also varies to ensure that the solar panel does not exceed its maximum power at high temperatures. You accomplish this task by reducing the input current to the battery at higher temperatures. Again, a cost-effective thermal-monitor circuit using BAT54 diodes provides feedback to adjust the output voltage and output current over the temperature range.

The design incorporates recovery from shading, overvoltage protection, dual-stage current regulation, and operation over a wide temperature range. Shading reduces the solar panel's output current and can force the solar panel, which has limited output-power capability, into an overload condition to the right of the knee shown in Figure 1. A National Semiconductor LM4041

TABLE 1 TEST DATA OVER THE OPERATING-TEMPERATURE RANGE

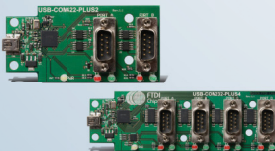
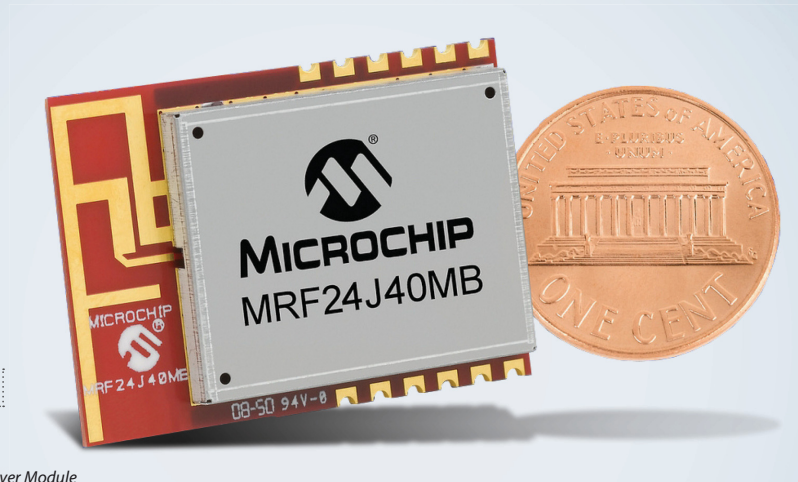
Temperature (°C)	Input voltage (V)	Input current (A)	SEPIC voltage (V)	Boost voltage (V)	Battery voltage with converter (V)	Battery current (A)	Efficiency (%)
25	9.2	0.198	9.2	13.14	12.84	0.098	69.08
30	9	0.193	8.9	13.2	12.64	0.095	69.13
40	8.6	0.187	8.3	13.35	12.6	0.088	68.95
50	8.2	0.178	7.7	13.51	12.56	0.08	68.84
60	7.8	0.216	7	13.66	12.58	0.095	70.93
65	7.6	0.208	6.7	13.75	12.56	0.09	71.51
70	7.4	0.204	6.4	13.84	12.56	0.084	69.89
80	7	0.192	5.8	14.01	12.51	0.075	69.81
90	6.6	0.177	5.2	14.19	12.48	0.067	71.58
100	6.2	0.165	4.5	14.32	12.45	0.055	66.94

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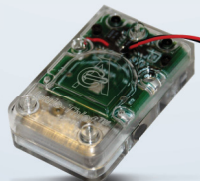
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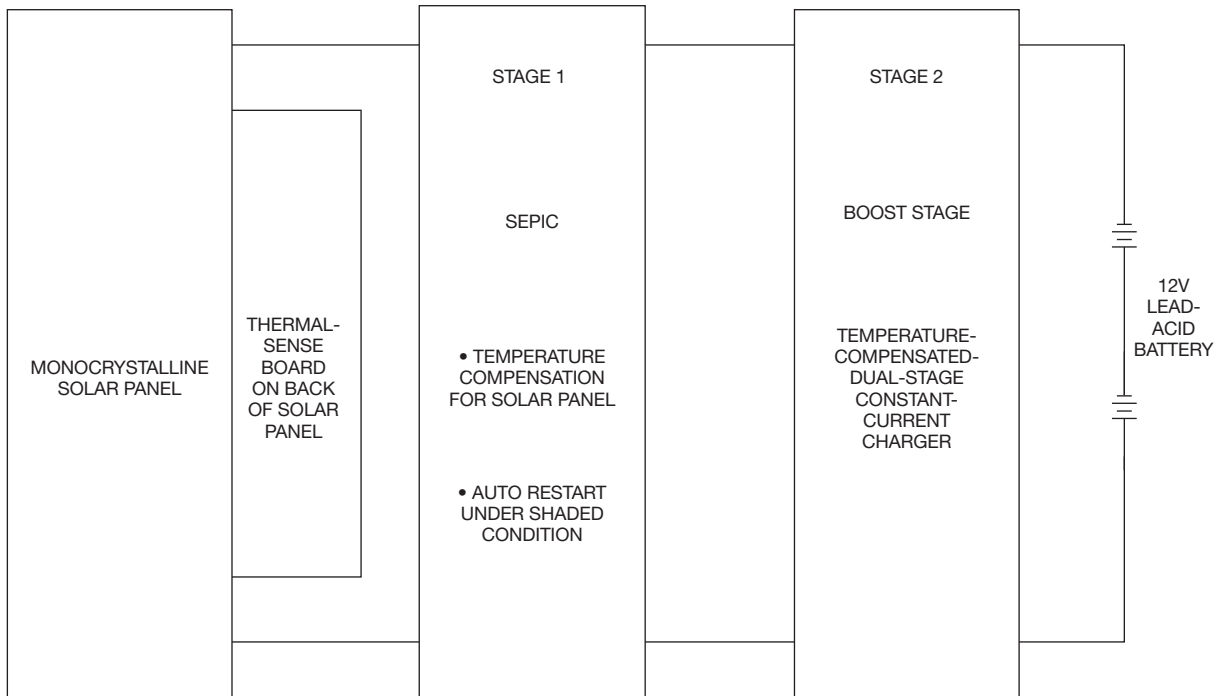


Figure 3 The solar charger system uses an 18-cell, 3W solar panel as the input source. The system comprises two stages, in which the first stage monitors the solar panel's voltages using a SEPIC topology and provides the output voltage, which tracks the input of the solar panel's voltage over the temperature range.

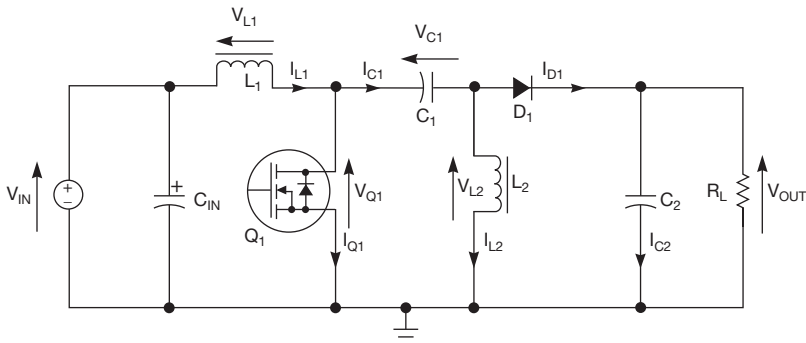


Figure 4 A SEPIC is a dc/dc topology that allows the output voltage to be greater than, less than, or equal to the input voltage.

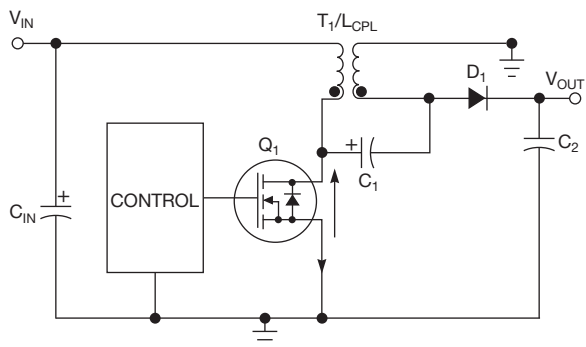


Figure 5 Replacing the inductor L_2 of Figure 4 yields an isolated SEPIC.

monitors the input voltage, and, if the input voltage decreases due to shading on the solar panel, the unit will undergo restart mode once you remove the shading-induced false condition.

Under full sunlight, the solar panel delivers 198 mA of current under loaded conditions at 25°C (Table 1). A shaded solar panel's current decreases to 30 mA, depending on the extent of the shading. This decrease forces the solar panel into an overload condition because the battery requires a higher current than the solar panel can deliver, and the solar panel's output voltage decreases from approximately 11V to less than 4V. The design incorporates dual-stage current regulation to provide optimum current under various temperature conditions.

Stage 1 of the design uses a SEPIC topology to take the output of the solar panel, which varies from 9V at 25°C to 6V at 100°C, as the input to the SEPIC. The SEPIC design uses a National Semiconductor LM5001 operating at 780 kHz. The solar panel has a negative-temperature coefficient of -2.2 mV/°C per cell. For a panel comprising 18 cells, that coefficient amounts to -39.6 mV/°C for an unloaded panel. This coefficient implies that the solar

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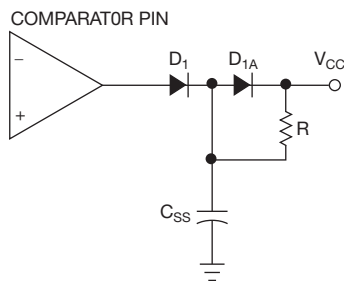


Figure 6 The design incorporates an external soft-start circuit to extend the soft-start time and ensure that the solar panel does not become overloaded during turn-on.

panel's voltage varies by $-40 \text{ mV}/^\circ\text{C}$. That is, if you get 9V at 25°C , then a variation of 75°C ($40 \text{ mV}/^\circ\text{C}$), or 3V will occur at 100°C .

A SEPIC is a dc/dc converter that allows the output voltage to be greater than, less than, or equal to the input voltage and provides an output voltage that is of the same polarity as the input voltage controlling the duty cycle of the control transistor (**Figure 4**).

In continuous mode—that is, when the input inductor current, I_{L1} —never falls to 0A—the average voltage across V_{C1} equals the input voltage, provided that the value of C_1 is large enough. You can easily visualize this operation because the average voltage across inductors L_1 and L_2 is 0V; the loop comprising V_{IN} , L_1 , C_1 , and L_2 highlights the fact that V_{C1} equals the input voltage. Because C_1 blocks dc current, the average current through capacitor C_1 and IC_1 is 0A. Thus, the average current through L_2 is the average load current and independent of input current.

Replacing inductor L_2 with a transformer yields an isolated version of a SEPIC. Using a coupled inductor—that is, a 1-to-1 transformer—in place of L_1 and L_2 makes the design more cost-effective and allows you to replace inductors L_1 and L_2 with one magnetic element. You can then redraw the schematic (**Figure 5**). Turning on Q_1 holds the positive C_1 terminal that connects to the drain of Q_1 at ground level, and 1-to-1 transformer T_1 induces a voltage equal to the input voltage at the junction of D_1 and C_1 . Thus, the voltage across capacitor C_1 equals the input voltage. The SEPIC can provide an output voltage that is greater than

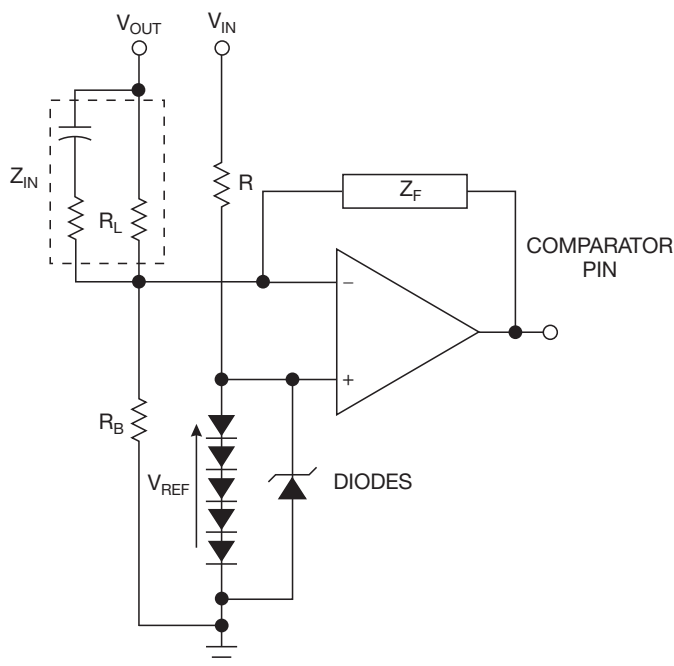


Figure 7 Changing the value of R_b adjusts the SEPIC voltage's setpoint to accommodate different solar panels' voltages. You can adjust a resistor divider comprising R_T and R_b to match the SEPIC's reference voltage, typically 1.34V at 25°C, which a thermal board generates.

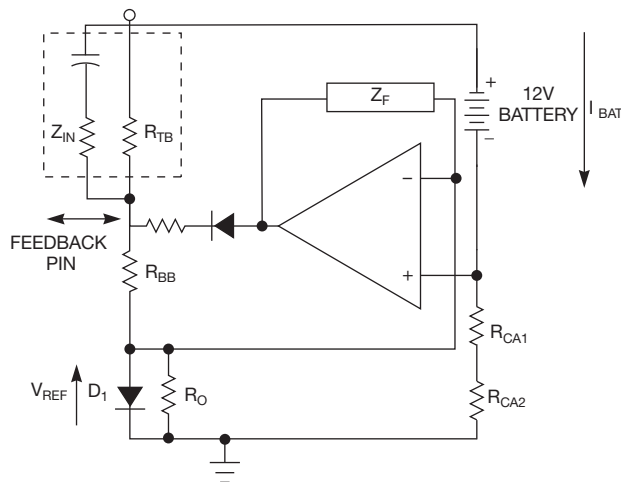


Figure 8 The second stage comprises a SEPIC that operates in boost mode with constant current-charge control and charges the 12V battery.

or less than the input voltage, according to the follow equation: $(V_{OUT}/V_{IN}) = D/(1-D)$, where V_{OUT} is the output voltage, V_{IN} is the input voltage, and D is the duty cycle of the main FET, Q_1 .

Because the solar panel has limited current-output capability, you must consider the inrush-current capability of the circuit. The LM5001 control element operates at 780 kHz, which de-

termines the internal soft start. The design incorporates an external soft-start circuit comprising D_I/D_{1A} , R , and soft-start capacitor, C_{SS} , to extend the soft-start time and ensure that the solar panel does not become overloaded during turn-on (**Figure 6**).

By changing the value of R_B in **Figure 7** to adjust the voltage divider in the first stage of the SEPIC, you can

adjust the SEPIC voltage's setpoint to accommodate different solar-panel voltages. You can adjust a resistor divider comprising R_T and R_B to match the SEPIC's reference voltage, typically 1.34V at 25°C, which the thermal board generates. A string of diodes generates a reference voltage that varies with temperature, thus providing temperature compensation to the design. The output of the first stage tracks the solar panel's voltage and adjusts for varying temperature. It is critical that the reference circuit comprising the string of diodes be close to the hot spot to track the temperature variation.

BATTERY-CHARGE CURRENT

The second stage of the design comprises a SEPIC that operates in boost mode with constant current-charge control.

This SEPIC charges the 12V battery (Figure 8). Adjusting the value of R_{CA1} and R_{CA2} allows the adjustment of the battery-charging current, I_{BAT} , by dividing the reference voltage, which diode $D_1 - V_{D1}$'s forward drop sets; a typical value is 0.183V at 25°C. You then divide the result by $R_{CA1} + R_{CA2}$. Because the reference voltage's drop, due to D_1 , varies with temperature, this calculation accounts for the battery's charging-current variation over temperature: $I_{BAT} = (V_{D1}) / (R_{CA1} + R_{CA2})$. You set the two-stage current charging by bypassing the R_{CA2} current-set resistor once the temperature reaches 60°C. Adjusting the R_{TB} and R_{BB} resistor values in Figure 8 sets the second-stage converter's boost voltage.

When the solar panel is in shade, its current capability decreases, resulting in overloading of the solar panel because of the fixed load on the solar panel; battery charging requires this fixed load. This overloading reduces the solar panel's output voltage. The R_{BR}/R_{TR} divider that connects to the LM4041 in the first stage senses the solar panel's output voltage, which initiates a restart mode by disabling the second stage of the circuit by pulling down on the enable pin of LM5001 (Figure 9).

Once you remove the fault condition that shading causes, the solar panel's voltage increases and allows the circuit to operate in the normal condition. The R_{BR}/R_{TR} divider senses when this voltage falls due to shading and rises again. The divider disables the second stage by pulling down the LM5001's enable pin.

BOOST OVERVOLTAGE PROTECTION

If you accidentally disconnect the thermal board that houses both diode D_1 in Figure 8 and diode string V_{REF} in Figure 7, the boost output voltage will clamp to a fixed output voltage, thus preventing the output voltage from exceeding a fixed, predetermined level and preventing any damage to the battery.

The following equation determines the maximum boost voltage in case of an accidental disconnection of the thermal board: $V_{BOOSTCLAMP} = [(R_0 + R_{TB} + R_{BB}) / (R_{BB} + R_0)] V_{REFLM5001}$, where the LM5001's reference voltage is nominally 1.26V,

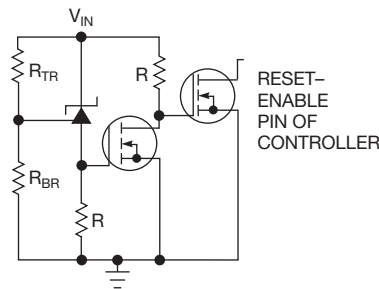


Figure 9 The R_{BR}/R_{TR} divider that connects to the LM4041 in the first stage senses the solar panel's output voltage, which initiates a restart mode by disabling the second stage of the circuit by pulling down on the enable pin of LM5001.

ensuring that the battery does not exceed its overvoltage limit.

Test data on the unit over temperature in the lab using a dc source shows the performance of the two-stage solar-charger circuit. Figure 10 shows the battery-charging current versus temperature, and Figure 11 shows the voltage from the solar panel versus the overall charger efficiency. Figure 12 shows the typical waveforms of the circuit, highlighting the battery-charging current, the output ripple, and the switch node's waveform.

At 60°C, the circuit moves into the second-stage current regulation, in which the current to the battery increases. The bolded text in column 7 in Table 1 highlights this transition point. This transition point provides optimum efficiency for the application because 60°C is the normal operating temperature for the application.

The solar-powered lead-acid battery charger connects to the battery using an industry-standard onboard-diagnostic-connector interface or another equivalent connection mechanism. You can adjust the design to accommodate various solar panels with different power and voltage ratings. You can also modify this cost-effective design to incorporate short-

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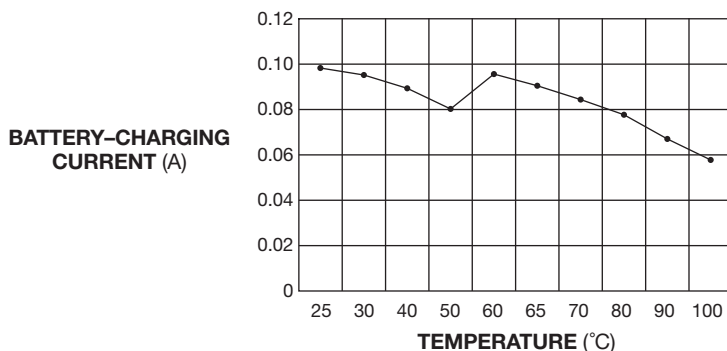


Figure 10 The normal operating temperature for the charger is 60°C.

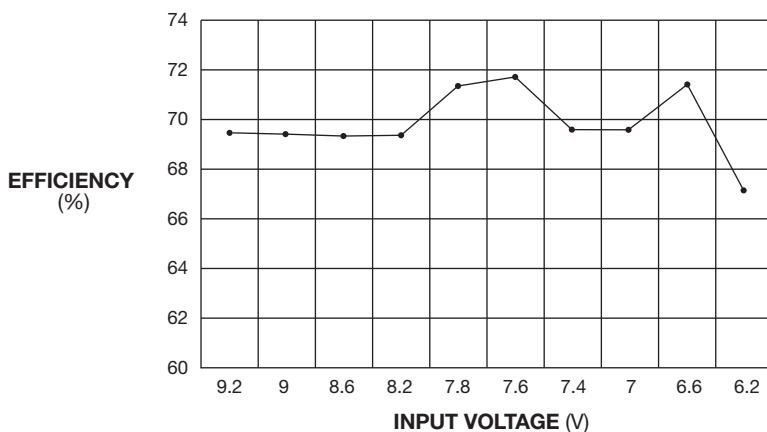


Figure 11 Efficiency falls off rapidly when the input voltage from the solar panel falls below 6.5V.

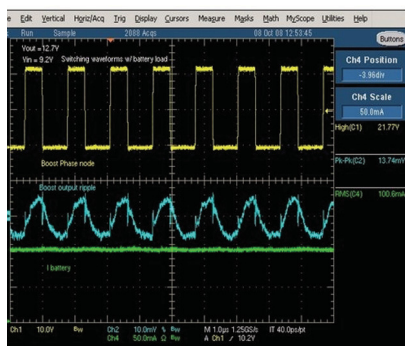


Figure 12 Typical converter waveforms highlight the battery load (top) and the boost output ripple current (bottom).

circuit protection with only three extra components. **EDN**

AUTHORS' BIOGRAPHIES

Ramesh Khanna is principal power-applications engineer at National Semiconductor, where he has worked for five years. In his current position, Khanna is responsible

for designing and developing systems for customers in the solar-energy, alternative-energy, power-over-Ethernet, LED-lighting, and other markets. He has more than 30 years of experience in ac/dc- and dc/dc-power-conversion design. Khanna has a bachelor's degree in engineering from Concordia University (Montreal, PQ, Canada) and a master's degree in engineering from the University of Colorado (Boulder, CO).

Frank Edrada is a power-application technician at National Semiconductor, where he has worked for five years. In his current position, Edrada manages the engineering lab, does PCB (printed-circuit-board) layouts for various system designs, assembles and tests PCBs, supports engineers on various designs, and performs troubleshooting by repairing various design circuits and writing documentation. He has associate's degrees in both electronics and electrical engineering.

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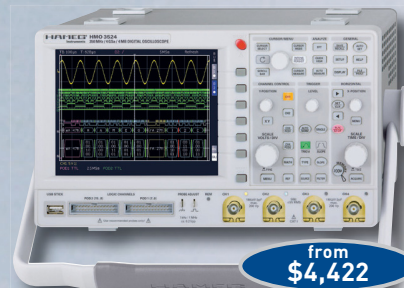
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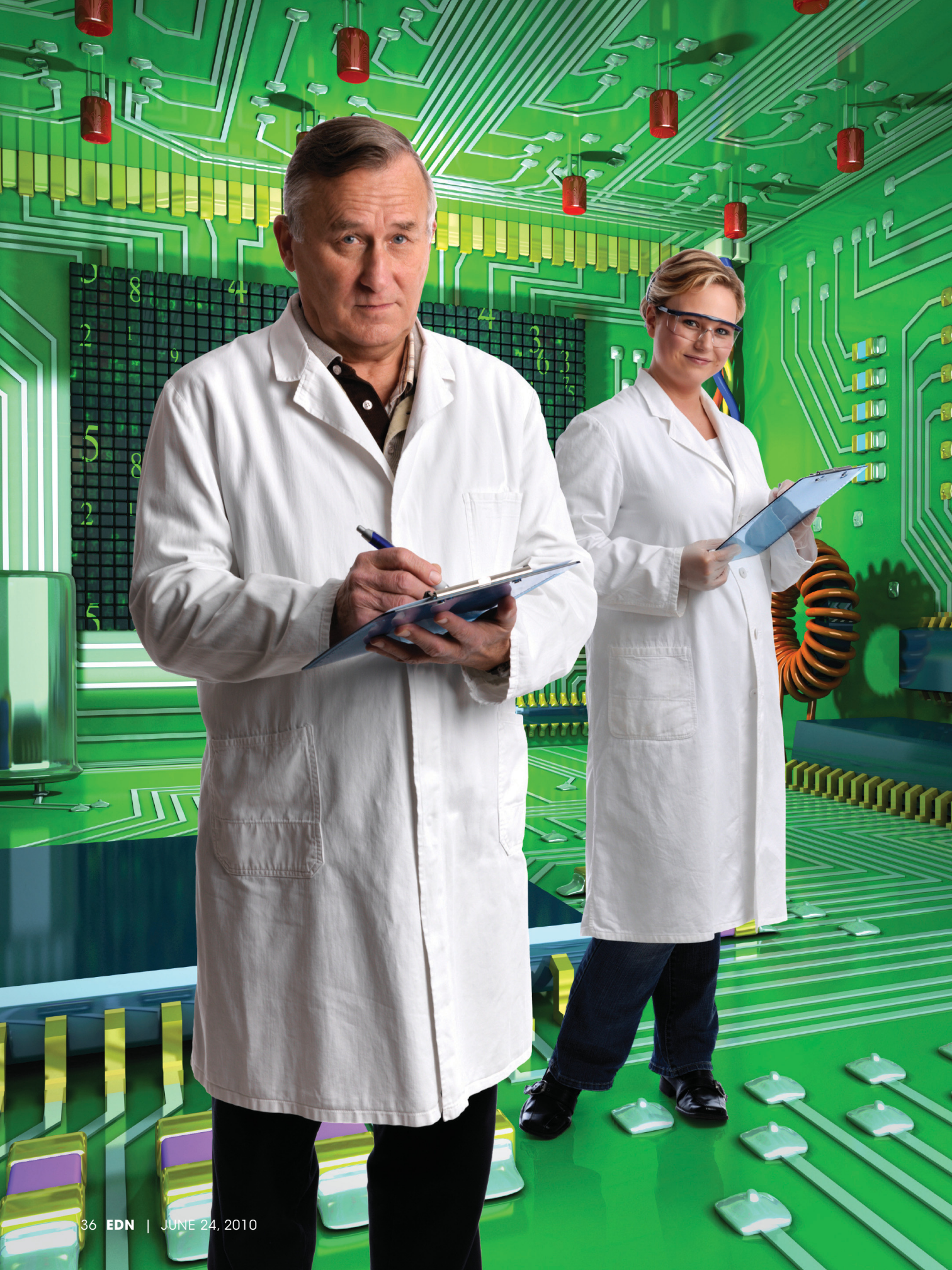


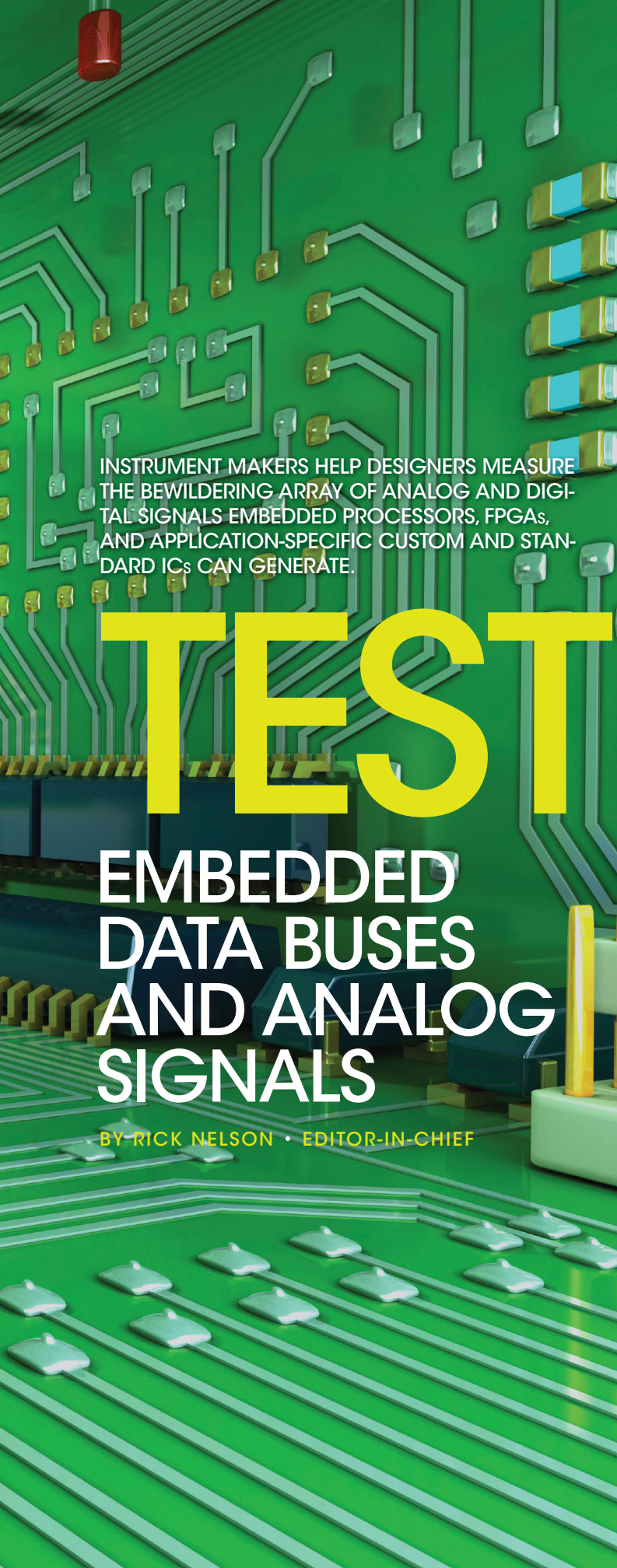
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EMBEDDED DATA BUSES AND ANALOG SIGNALS

BY RICK NELSON • EDITOR-IN-CHIEF

Embedded computers are finding their way into products ranging from automobiles and aircraft to mobile devices and tabletop consumer appliances. Designers working in the embedded market face many challenges in selecting the right processor or microcontroller and software. They must then demonstrate that the product they design works. If it doesn't work, they need to pinpoint the cause of failure and provide a fix. To help designers accomplish that goal, test-and-measurement companies are offering a variety of instruments, including oscilloscopes, logic analyzers, and protocol analyzers. In addition, software companies are making test-software suites that can put a product through its paces and ensure that it will meet customer expectations.

The ESC (Embedded Systems Conference) Silicon Valley, which took place in San Jose, CA, in April, provided test-and-measurement companies an opportunity to highlight their offerings for the embedded-system market. Test-related products on display ranged from traditional oscilloscopes through logic analyzers, protocol analyzers, and software as vendors tried to attract customers who are designing processors, FPGAs, and other components into their embedded systems.

Tektronix showcased mixed-signal oscilloscopes at ESC, presenting the results of a time-and-motion study it sponsored that demonstrated how long it takes engineers to find runs and glitches when debugging designs. According to the study, users perform typical debugging tasks 53% faster when using Tektronix scopes, such as the MSO4000 mixed-signal oscilloscope (Figure 1), than with competitors' versions.

SERIAL AND PARALLEL BUSES

"We know from our own research that 60% of oscilloscope users are working with serial buses today and 50% are working with parallel buses," says Gina Maria Bonini, technical-marketing manager at Tektronix. With users' emphasis on digital debugging, Tektronix wanted to know how efficiently its scopes could support customers compared with competitors' scopes selling for \$19,000 to \$21,000, she adds. Toward that

end, Tektronix commissioned Hansa GCR to conduct in-person interviews with 47 experienced oscilloscope users, asking them to complete the same debugging task.

"This directional research indicated that users were able to find runts and glitches in a signal twice as fast with the Tektronix oscilloscope compared to the Agilent and LeCroy scopes," says Andrea Eaker, senior research consultant at Hansa GCR. "Users also found the automated search feature and available triggers particularly useful in completing these tasks, and Tektronix received the highest satisfaction ratings overall."

The study asked the participants to set up each oscilloscope to monitor for glitches and runts, set up a trigger and capture a runt, and search the waveform to locate all runt instances. According to Bonini, the ability to quickly perform those steps helps users pinpoint signal-integrity problems that relate to timing errors, bus-contention issues, metastability, setup-and-hold violations, and various physical-layer issues involving termination and other problems.

Bonini attributes the Tektronix scopes' performance in the study to the company's digital-phosphor technology, which enables the capture of 50,000 waveforms/sec. "With the digital-phosphor technology, we overlay waveform after waveform to try to duplicate the analog-scope experience so that users can see when there are anomalies in a signal,"

AT A GLANCE

Automated search assists scope users in deciphering 10 million-point signal acquisitions.

Hot topics at DesignCon one year become hot topics at the ESC (Embedded Systems Conference) a few years later.

FPGAs, serial buses, and DDR memory are increasingly driving embedded designs.

MSOs (mixed-signal oscilloscopes) will complement—not replace—logic analyzers.

The computer industry drives down the price of technology so that it becomes feasible for embedded designs.

she says. The MSO4000 also has an automated-search feature that is useful for long-record oscilloscopes that can perform 10 million-point acquisitions, representing 10,000 screens of data. With the MSO4000, a user can set up a runt trigger and leave the oscilloscope running overnight or over a weekend, looking for metastability or other problems.

EMBEDDED-TEST TOOLS

Dan Monopoli and William Driver, product-marketing managers at LeCroy, describe the types of instruments and capabilities embedded-system designers—versus designers in other areas—

are looking for. LeCroy customers are in two broad camps: those who attend ESC and those who attend DesignCon. Although both Monopoli and Driver attended ESC, the show tends to be the domain of Monopoli, who is primarily responsible for products that operate as fast as 1 GHz. DesignCon, on the other hand, is more the domain of Driver, who is primarily responsible for products in the 1- to 6-GHz range.

According to Monopoli, customers at ESC are looking for instruments that can handle decoding for I²C (inter-integrated-circuit), SPI (serial-peripheral-interface), and UART (universal-asynchronous-transmitter/receiver) signals. In contrast, DesignCon attendees are looking for high-bandwidth scopes that can help investigate signal-integrity issues on high-speed buses, such as USB 3 and PCIe Generation 3. DesignCon attendees are early adopters who are bringing up new silicon or perhaps don't even have silicon yet but are preparing to make measurements when it does arrive.

LeCroy exhibited 6- and 30-GHz scopes at ESC to demonstrate the company's broad product lineup, but Driver says that he answered more questions about Monopoli's product lineup than about his own. Having high-end instruments at ESC gave the company the chance to demonstrate the consistent options, capabilities, and interfaces across the full lineup of instruments, Driver explains.

Monopoli says that this year's ESC Silicon Valley attendees were not looking for high bandwidth or tremendous memory depth but rather extensive measurement capabilities that would enable them to handle mixed-signal circuits as well as I²C, SPI, and, increasingly, CAN (controller-area-network) buses, which are finding use beyond traditional automotive applications. Prospective customers also want all these capabilities at an attractive price that will enable them to get prompt purchase approval. A hot topic at DesignCon one year, he says, will turn out to be a hot topic at ESC a few years later as prices for new technology fall to a point at which it can serve in embedded-system applications (see sidebar "Opportunity at the edge").

At ESC, LeCroy introduced its ArbStudio AWGs (arbitrary-waveform

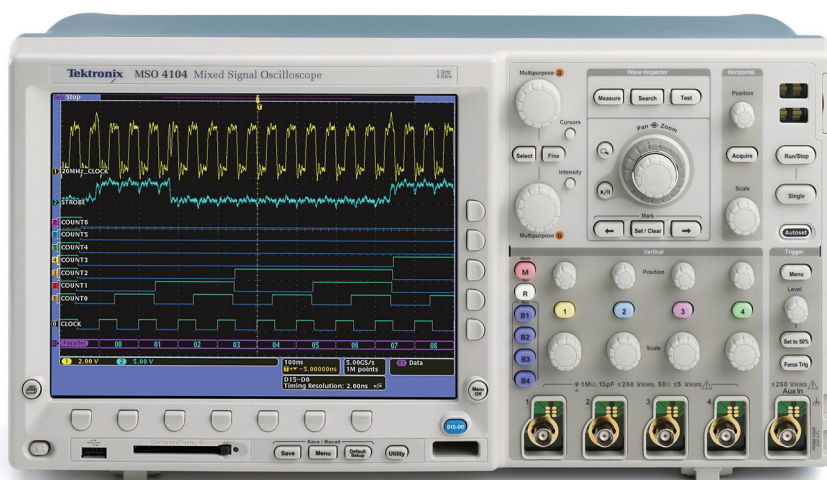
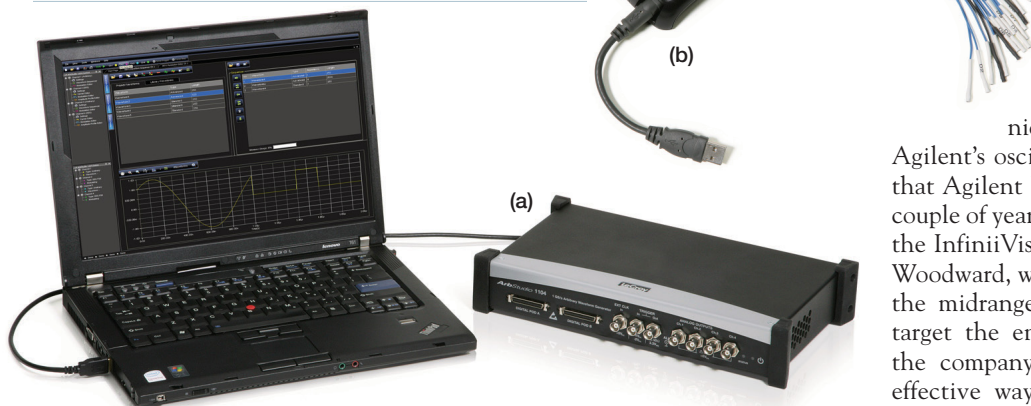


Figure 1 Mixed-signal oscilloscopes, such as the Tektronix MSO4000, have become key embedded-system test tools. Tektronix commissioned a study by Hansa GCR, which concluded that engineers can find runts and glitches twice as fast with the Tektronix scope as with competitive scopes.

Figure 2 LeCroy's ArbStudio AWGs generate signals as fast as 125 MHz and include PWM capabilities. ArbStudio software runs on an external PC (a). The LogicStudio 16 brings logic-analyzer functions to a PC (b).



generators) and LogicStudio 16 logic analyzer. The ArbStudio AWGs (**Figure 2a**) generate signals as fast as 125 MHz and include PWM (pulse-width-modulation) capabilities. The software interface that controls the hardware simplifies waveform creation with a navigation tree that allows easy access to all channels.

The ArbStudio series includes four models: two- and four-channel versions with analog waveform capabilities plus two- and four-channel versions offering a combination of analog waveform and digital pattern-generation capabilities that Monopoli describes as the AWG versions of mixed-signal oscilloscopes. The four-channel models have an expansion port that allows you to connect as many as eight units. All models have a 125-MHz bandwidth, 1G-sample/sec maximum sample rate, 2 million-point/channel memory, and 16-bit resolution. The instruments support both true arbitrary and DDS (direct-digital-synthesis) technologies. ArbStudio software runs on an external PC. According to Monopoli, LeCroy chose ESC for the introduction because it well fits the embedded-system-test niche with an attractive less-than-\$5000 price. Prices for the models range from \$2490 to \$4990.

LeCroy also debuted at ESC its LogicStudio 16 (**Figure 2b**), which brings logic-analyzer functions to a PC, providing 16 channels with a sample rate of 1G sample/sec and maximum input frequency as great as 100 MHz. LogicStudio 16 software provides a dynamic waveform display with an intuitive

user interface. Tools for digital debugging include timing cursors, zooming and panning functions, a persistence display, and a history mode that can replay old data captures. LogicStudio supports protocol analysis for I²C, SPI, and UART interfaces. It can trigger on specific bus addresses or data packets. With a \$990 price, the LogicStudio 16 is neither the most expensive nor the least expensive USB logic analyzer in its class, says Monopoli. A key benefit is that LogicStudio provides a communication link to LeCroy's WaveJet oscilloscope, thereby turning a PC in to a mixed-signal debugging environment.

WEB RELIANCE

One company conspicuous in its absence from ESC was Agilent Technologies, the largest test-and-measurement company. Joel Woodward, senior product manager for Agilent's oscilloscope group, explains that Agilent last exhibited products a couple of years ago when it introduced the InfiniiVision 7000. However, says Woodward, who also is responsible for the midrange Infinii models that target the embedded-system market, the company has found more cost-effective ways—primarily, the Internet—to reach prospective customers. He cites the increasing tendency to build Web servers into instruments, enabling prospective customers to remotely testdrive them and get a full demonstration without attending a trade show.

If Agilent had exhibited products, Woodward says, he would have demonstrated the company's logic analyzers and oscilloscopes as they apply to three technologies, each of which applies to multiple markets. The company would also have highlighted its probing technology (**Figure 3**). After all, Agilent's instruments can't measure signals if there's no way to access them on the board under test.

OPPORTUNITY AT THE EDGE

Edge devices—ranging from sensors to cell phones—are promising to capture significant investment as the electronics industry rebounds from recession, according to Greg Peters, vice president and general manager of the component-test division of Agilent Technologies. Speaking May 25 at a press conference at the International Microwave Symposium (www.ims2010.org), Peters described edge devices as products that touch the real world. He said that investment is increasingly moving from the core—computers or servers in back rooms—to the edge, with edge devices accounting for billions of dollars in sales. Applications include security, health, and environmental monitoring, with medical applications for portable or surgically implanted devices increasing rapidly.

The engineers building systems of edge devices will be experts in their application area, Peters said, not in electronics—which is simply the tool they need to get the job done. In addition, the proliferation of wireless sensors will drive bandwidth requirements. To address the core-to-edge trend from a test-equipment perspective, Agilent is offering handheld RF-network and spectrum analyzers, including a new two-port version with built-in calibration.

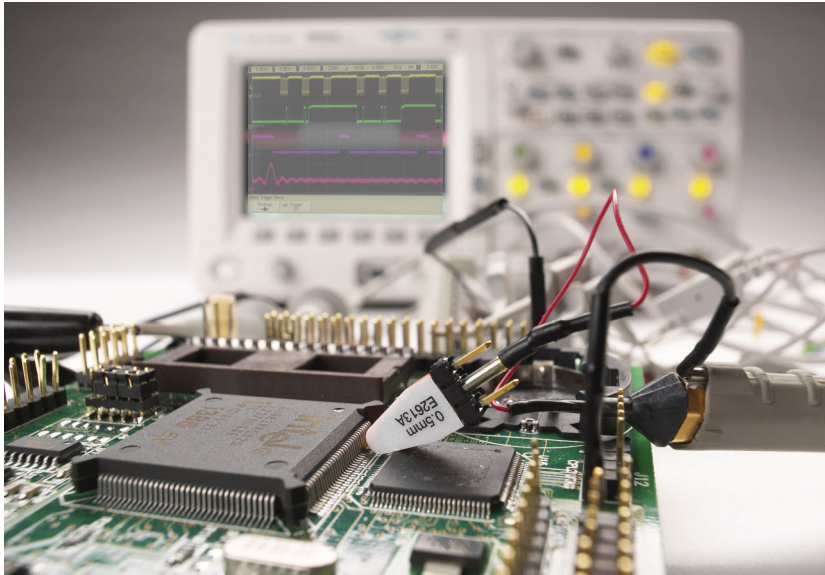


Figure 3 The two test points for probe attachment may sometimes be inconveniently far apart. Agilent's wedge probe adapter provides hands-free, mechanically noninvasive contact to fine-pitch IC pins in embedded-system boards.

Agilent would choose to highlight its technology that employs FPGAs, which have grown to a \$3 billion market from the niche market they constituted in the early 1990s. Woodward says that FPGAs are often the centerpieces of embedded designs for medical, consumer, industrial, aerospace and defense, and even mobile-computing markets. Agilent serves designers of embedded systems incorporating FPGAs by offering dynamic-probe technology that lets designers incrementally peer into FPGAs, seeing additional sets of signals with a few mouse clicks.

If Agilent had attended ESC, it would also have addressed memory and serial-bus technologies. "DDR memory has really taken hold in the embedded market, and a lot of embedded development teams using DDR memory have acute needs for validating and debugging their memory solutions," Woodward says. These products include oscilloscopes and logic analyzers for physical- and protocol-layer analysis. He concurs with his counterparts at LeCroy and Tektronix on the ubiquity of serial buses, such as lower-speed buses I²C and SPI. High-speed buses are also appearing in

embedded designs (**Figure 4**). Agilent also offers approximately 20 protocol-analysis products, many in conjunction with its oscilloscopes.

SOFTWARE APPROACHES

Not all test products on exhibit at ESC were test instruments. For example, Koizio representatives were on hand to highlight the company's software for design validation, manufacturing test, and in-field test. The company offers a suite of software tools for embedded

systems. According to Joseph Skazinski, co-founder and chief business-development officer at the company, the software provides broad datapath coverage and standardized diagnostic tests across functional areas. It also supports fast, automatic troubleshooting, giving users maximum control. Skazinski says that customers can save \$100,000 in test development and debugging costs per project and achieve a three-month reduction in time to market.

The Koizio suite helps PCB (printed-circuit-board) designers contend with increasingly complex boards. Skazinski cites Mentor Graphics figures showing that average board sizes have decreased over the last 15 years from 101 to 75 in.². Component counts, however, have increased from 649 to 3399, component pins have increased from 4214 to 13,505, and the number of pin-to-pin connections has increased 5190 to 10,960. Meanwhile, designers are contending with tight schedules, limited resources, design and manufacturing silos, and the need to deal with remote teams.

For design validation, the tools support interactive hardware debugging, fault isolation, characterization, and regression testing. For manufacturing test, they support parallel test and IP (intellectual-property) protection, and contract manufacturers can adapt them. In the field, the tools support built-in self-test and diagnostics. The tools provide coverage of memory, data buses, user interfaces, displays, and cameras, as well as audio, networking, and wireless functions.

Koizio's recent product introductions include an expansion of its Diagnostics Design Suite in-system diagnostics software to support the PowerPC 460GTx and 460 SX storage processors from Applied Micro Circuits. Koizio's tool provides at-speed functional tests with interactive and automated interfaces. This year, the company announced support for the new OMAP (Open Multimedia Applications Platform) 4 from Texas Instruments.

If you are looking to embed instrument capability into your systems, you might consider the line of board-level backplanes that National Instruments in-

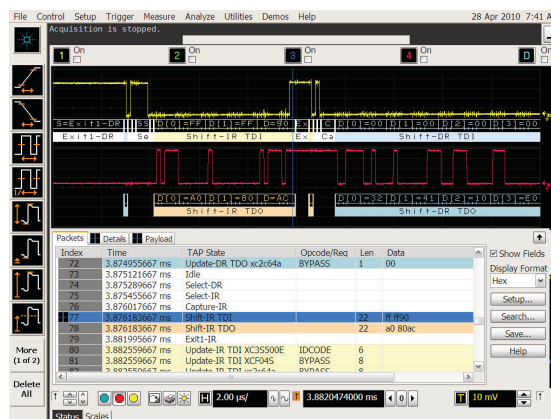


Figure 4 Serial buses often provide key debugging access points. Agilent's Infiniium series oscilloscopes provide protocol-level triggering and decoding for more than 15 serial buses ranging from I²C to PCIe. Agilent's newest protocol-decoding application supports JTAG, or IEEE 1149.1.

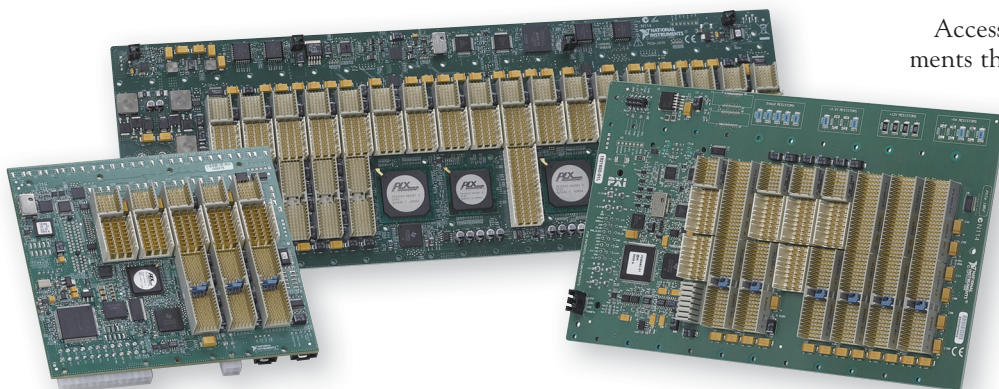


Figure 5 Board-level backplanes, previously available only as part of National Instruments' PXI/CompactPCI and PXIe chassis, allow OEMs to create their own custom rugged enclosures, which can accommodate PXI, PXIe, CompactPCI, and CompactPCIe modules.

troduced at ESC (**Figure 5**). The new backplanes, previously available only as part of NI's PXI (PCI extensions for instrumentation)/CompactPCI (Peripheral Component Interconnect) and PXIe (PXI Express) chassis, allow OEMs to create their own custom, rugged enclosures that can accommodate PXI, PXIe, CompactPCI, and CompactPCIe (PCI Express) modules.

The more than 10 new 3U and 6U backplanes offer four to 18 slots. Engineers can design custom installations and enclosures around the backplanes and integrate more than 1500 PXI modules, including data-acquisition cards; FPGA-based I/O modules; high-end instruments, such as signal generators and RF-signal analyzers; and a variety of bus-interface modules, including serial, MIL-STD (military-standard)-1553, IEEE 1588, Profibus, and DeviceNet versions.

Designers can use the NI LabView graphical-system-design platform to design, prototype, and deploy all aspects

of their systems, in keeping with what Casey Weltzin, LabView real-time product manager at NI, describes as a focus on letting domain experts in robotics, medical, and energy industries, for example, take a large role in embedded-system designs.

EMBEDDED TEST'S FUTURE

You can expect instrumentation offerings to continue to evolve as vendors develop strategies to help their customers contend with embedded-system designs, but don't expect the demise of any instruments or the emergence of drastically new ones. The industry has seen the decline of some classes of instrumentation. Agilent's Woodward points out that board-level emulators, for example, have declined because you can get the functionality of a \$30 emulator board for a nickel's worth of on-processor silicon.

The emergence of MSOs (mixed-signal oscilloscopes) might suggest that they will put logic analyzers on a path to follow board-level emulators, but vendors of both classes of instruments don't expect that scenario to happen. Tektronix's Bonini says that the logic analyzer will remain the tool of choice for logic designers who need to dig deep into protocol layers to troubleshoot designs with multiple buses. For logic-analyzer users who need to look at analog effects, Tektronix offers a multiplexer within its logic analyzers that can route signals to an oscilloscope without the inconvenience and loading effects of trying to attach two probes to a circuit node of interest.

Access to serial buses and instruments that can decode the bus protocols will become increasingly important to embedded-system test as circuitry becomes ever more complex. "As the many design blocks in embedded systems continue to get integrated into ever-more-dense ICs, such as FPGAs, ASICs, and ASSPs [application-specific standard products], our experience has been that the serial-communications buses between blocks don't disappear," says Woodward. "Often, they are the only means of access for a design team to get information on what's happening in its design."

Increasingly, those buses will be high-speed, and you can expect a decrease in the time delay between when a bus represents a hot topic at DesignCon and when it's a hot topic at ESC, as Monopoli describes. Woodward notes that the cost of high-speed serial SERDES (serializer/deserializer) buses isn't that daunting. If you buy a modern FPGA, it is essentially free.

"People in the medical industry have embraced high-speed serial buses," says Woodward. "In MRI [magnetic-resonance imaging], the buses can move large amounts of graphics data from one subsystem in a design to another subsystem. A lot of times, we think of embedded as a lagging industry, but embedded has wholeheartedly embraced the adoption of high-speed serial links. I think FPGAs are driving a big part of that. You'll also find a number of ASSPs that have begun incorporating these high-speed transceivers that are also priced so that they work in the embedded market. The wonderful thing about the computer industry is it will drive the price of advanced technology down so it becomes feasible for embedded teams to implement them in their designs." **EDN**

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Dynamic and static CMR: impacts to signal integrity

OPTOCOUPLERS CAN PROTECT SYSTEMS AND USERS FROM HIGH-VOLTAGE SURGES. THEY CAN ALSO REJECT HIGH COMMON-MODE TRANSIENT NOISE THAT WOULD OTHERWISE RESULT IN ABNORMAL VOLTAGE TRANSITIONS OR EXCESSIVE NOISE ON THE OUTPUT SIGNAL.

Noise can have many sources. It can, for example, come from nearby electric fields' capacitive coupling, magnetic fields' inductive coupling, or conductive coupling due to differences in ground potentials. To combat this noise, devices often use CMR (common-mode rejection) to reject signals that are common to the input. This parameter is important especially in noisy environments because noise appears as offset in the inputs. The ability of a device to attenuate the noise and to transmit signals across it is important for signal integrity.

The key factors that determine the CMR performance of a device are common-mode voltage and common-mode transient noise. When the common-mode noise voltage is larger than the interface's input range or the input common-mode voltage's rejection range, you must use galvanic isolation. The switching current that causes voltages to spike often generates common-mode transient noise, which you define using the voltage and the rate of change. You must filter both common-mode noise and transient noise to ensure that the input signal does not become corrupt.

THE ISOLATOR'S ROLE

An isolator connects two electrical modules within a system to ensure that the system can transmit signals without a physical connection to the destination. Light is the most common mode through which you can transmit a signal within an isolator. In this case, you use an optocoupler as an isolator not only to protect systems and users from

high-voltage surges but also to reject high common-mode transient noise to either set of floating points, which otherwise may result in abnormal voltage transitions or excessive noise on the output signal.

The key parameter that measures the success of rejecting common-mode signals in an isolator is the common-mode current during a voltage transient. The following **equation** defines the common-mode current: $I_{CM} = C(dV/dt)$, where C is the parasitic capacitances due to packaging—pin-to-pin leadframe or wirebond leadframe, for example—and capacitance at the signal-coupling interface between the LED and the detector and dV/dt is the rate of the transient-voltage signal. This **equation** assumes that external factors, such as PCB (printed-circuit-board) layout or component placement, are optimized and contribute little parasitic capacitance.

To reduce the common-mode current, it is important to reduce these parasitic capacitances. The large separation between the LED and the photodetector—0.08 to 1 mm in a representative part, such as Avago's (www.avago.com)

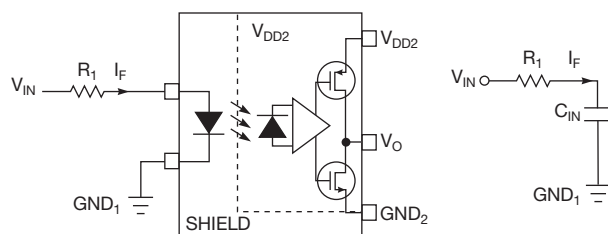


Figure 1 Current-limiting resistor R_1 and the LED's parasitic input capacitance act as a lowpass filter to high-frequency noise.

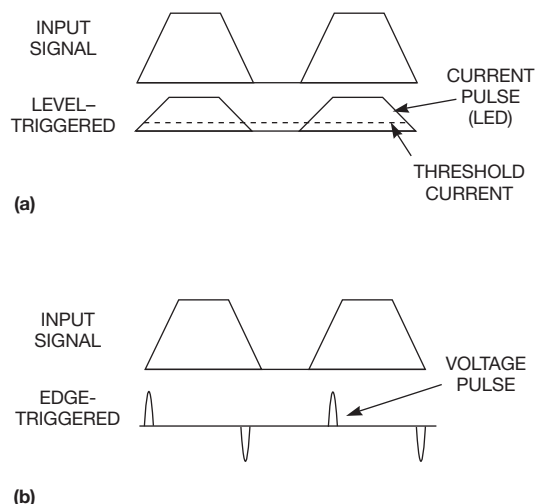


Figure 2 Optocouplers have either a level- (a) or an edge-triggered coding scheme (b).

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ACPL-J313—minimizes the parasitic capacitance and thus results in small leakage current during common-mode transients. The part also has a built-in proprietary Faraday shield between the input LED and the photodiode to provide increased common-mode noise rejection.

This internal transparent, conductive shield allows optical coupling to the photodiode but diverts electrically coupled current to the ground pin, improving the parasitic capacitance, which in turn improves the CMR of the optocoupler. In addition, this shield helps to discharge the charges that accumulate on the detector chip due to large common-mode voltage that is applied across the device for a substantial period of time. The ACPL-J313 can improve CMR performance by as much as 40 kV/ μ sec at 1.5-kV common-mode voltage.

On the other hand, a design in which the microcontroller is far away from the isolation interface and which thus has long wire traces, can easily pick up inductive noise and corrupt the signal. In this case, a direct-drive optocoupler, such as the ACPL-M61L, acts as a “natural” filter. A resistor is required to limit the current that drives the LED in an optocoupler (Figure 1). Together with the intrinsic input capacitance of the LED, the resistor/capacitor pair acts as a lowpass RC filter to shunt away the high-frequency noise.

STATIC AND DYNAMIC CMR

An isolator has both static and dynamic CMR. Static CMR is the signal-rejection capability when the input is static at either a logic high or a logic low. This situation usually occurs when the system is in the idle, or standby, state. During this state, some parts of the system are turned off to save power, leaving certain modules on to detect the input signal. The system must maintain and hold at the same logic regardless of the static common-mode noise in the environment. This requirement ensures that the noise does not falsely trigger the system.

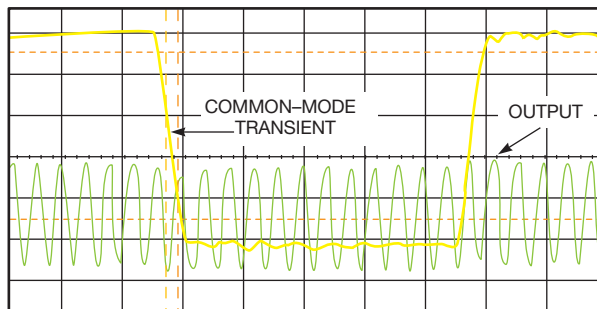


Figure 3 The ACPL-072L can withstand a 10-kV/ μ sec dynamic-CMR surge at a 25-Mbps signal rate. The yellow trace denotes the common-mode transient, and the green trace denotes the output signal. The ACPL-072L rejects the dynamic CMR to preserve signal integrity.

TYPICALLY, THE DYNAMIC CMR OF A SYSTEM IS WORSE THAN THE STATIC CMR, AND THE CMR CAPABILITY IS WORSE AT HIGHER COMMON-MODE VOLTAGES FOR DC VOLTAGE.

In a dynamic environment, the system transmits a signal that toggles between logic high and logic low. To prevent the common-mode noise from corrupting the input signal, the system must filter the noise using dynamic CMR. Typically, the dynamic CMR, or ac voltage, of a system is worse than the static CMR, or dc voltage, and the CMR capability is worse at higher common-mode voltages for dc voltage.

Dynamic CMR ensures that the system does not lose signals during operating mode. During this mode, most parts of the system are operating, and any erroneous signal the system transmits will cause the connect-

ing devices to erroneously turn on or off. This situation may result in a short circuit; overheating; or the destruction of expensive devices, such as motors and machines.

REJECTING COMMON-MODE TRANSIENTS

Some optocouplers adopt a level-triggered coding scheme. In this scheme, the LED detects the level of forward current the input signal sets and pulses the light output to the detector. In contrast, an edge-triggered coding scheme adopted in other isolators generates small voltage pulses during the transition edge of the input signal (Figure 2).

The duration of the current or voltage pulses is 100 nsec, for example, in a level-triggered coding scheme, such as that in an Avago ACPL-072L. As such, dynamic transient noise is less likely to corrupt the signal in these systems than in edge-triggered coding schemes, in which these pulses last 2 to 3 nsec. Due to the short rise and fall times of the LED current, the dynamic transient noise will probably result in a slight increase or decrease of pulse-width distortion in the level-triggered coding scheme. The edge-triggered scheme, in contrast, can possibly momentarily miss pulses. In short, optocouplers with level-triggered coding have inherently better dynamic-CMR performance.

Figure 3 shows the dynamic-CMR performance of a level-triggered optocoupler—the ACPL-072L—that can withstand a 10-kV/ μ sec dynamic-CMR surge at a 25-Mbps signal rate, rejecting the dynamic CMR to preserve signal integrity. **EDN**

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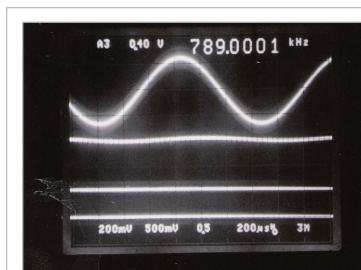



Figure 2 You feed the circuit an input tone (top trace) and get the output signal from the MSHN5 (second trace). The third and fourth traces represent the clock signal from the 74HC4046 PLL.

notch filters. When you tie the FSEL pin high, it selects notch; tying TYPE to AGND selects the narrow notch filter. This step ensures the removal of only one tone from the input signal with little information loss. IC₃'s 1000-to-1 clock-to-corner ratio reduces the chance that aliasing signals will affect the output. For voice applications, for example, no signals of 500 kHz or higher would be available to alias into the passband. A sample setup uses an input frequency of 789.13 Hz at a clock frequency of 789.13 kHz, 1000 times the input signal (**Figure 2**). The PLL tracks the input, moving the notch filter to 1.24 kHz. **EDN**

Image-capture system uses USB and LabView

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 Capturing and processing graphical images requires manipulating data into a form that you can use. This Design Idea describes an imaging system using a USB (Universal Serial Bus) image-capturing system that uses OmniVision's (www.ovt.com) 640×480-pixel, 8-bit-color OV7660 image sensor. The CY7C68013A-128AXC from Cypress Semiconductor (www.cypress.com) provides a USB interface between a PC and the image sensor (**Figure 1**). The control software is written in LabView from National Instruments (www.ni.com/labview).

To avoid losing data from the image sensor, the system employs a data buffer in the image-processing algorithm. The buffer uses system memory for data storage. The queue ensures that the system will not lose data regardless of how much time it takes to process each row in an image. This technique is useful in measurement systems in which the speed of data acquisition and data processing may differ.

Figure 2 shows the programming flow chart. After the system starts, you must set the driver to NI-VISA (Virtual Instru-

ment Software Architecture), a software layer that provides a common programming interface across many types of measurement instruments and software drivers. Once you set the driver, you can initiate the USB device. LabView provides a driver wizard that helps you to build drivers. The LabView code for this graphic-system design can easily implant USB data transmission and its applications. You can download the LabView code from the online version of this Design Idea at www.edn.com/100624dia.

After initializing the USB device, the software allocates system memory in a FIFO (first-in/first out) configuration to become the data buffer. A memory endpoint sets the input buffer's size to 4 kbytes. The software then reads the image in rows and stores data from the sensor in the buffer memory. After reading the data from the buffer, the system image uses two threads to process the data.

Figure 3, available with the online version of this Design Idea at www.edn.com/100624dia, shows the LabView programming diagram for USB data transmission. The program includes for-loop pro-

cedures for storing the image in the buffer memory, reading and processing image data, and performing state checking.

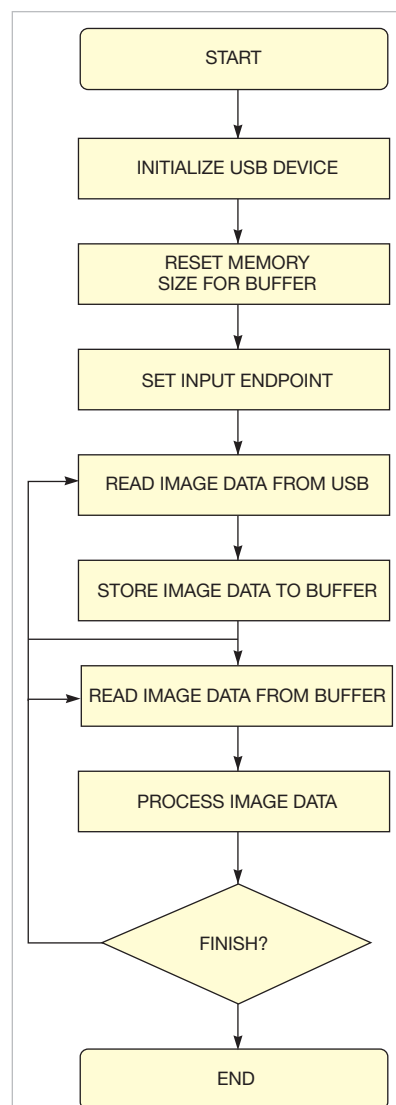


Figure 2 This algorithm lets a host PC capture data from the image sensor.

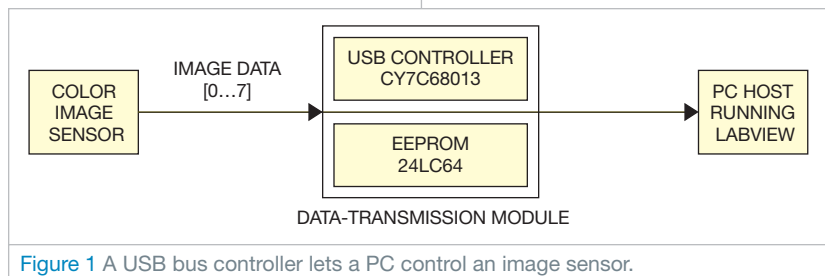
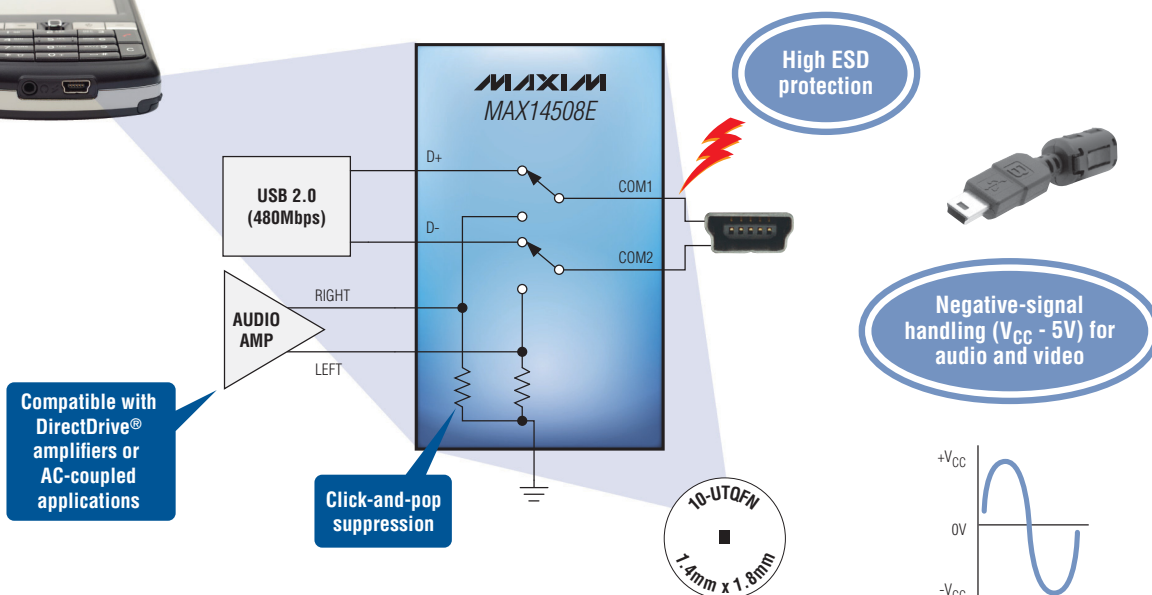


Figure 1 A USB bus controller lets a PC control an image sensor.



Tiny, Hi-Speed USB/audio/video switches enable single connector



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- High 950MHz bandwidth (video)

Save board space

- Allow interfacing to small USB connectors

Part	Configuration	Supply Voltage (V)	V _{BUS} Detection/Enable	Fault Protection	Shunt Resistors
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MAX14509E*			Enable		
MAX14509AE			V _{BUS}		✓
MAX14510E*			V _{BUS}		

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*Future product—contact factory for availability.

EV kit available

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The main processing algorithm obtains and displays red, green, and blue data of each pixel. **Figure 4**, available with the online version of this Design

Idea at www.edn.com/100624dia, shows the test result. The element in the buffer shows that the system processed 614,400 pixels. The actual amount will

vary based on the PC's performance. A powerful PC can smoothly run this program, whereas a weak PC will cause the data to accumulate in the buffer. **EDN**

Low-cost RF synthesizer uses generic ICs

James B Wood, Inovonics Inc, Felton, CA

 You can design a hardware-based frequency synthesizer with one inexpensive IC and a few passive components. Such synthesizer chips are not always available, however, because they are typically single-sourced and are not in stock with parts distributors. The need for a working circuit in a short time and using common parts prompted the creation of the circuit in this Design Idea. The synthesizer covers the US commercial AM (amplitude-modulation) broadcast band. It tunes in 10-kHz steps from 500 to 1800 kHz, but you can scale the

frequencies for other applications.

The PLL (phase-locked loop) time base is a 100-kHz, tuning-fork-cut crystal of the same size as those in wrist watches. Using a more common crystal requires some extra parts to scale the frequency. Note that if you attempt to use one of these tiny crystals with a CMOS-gate oscillator circuit, however, the circuit will either fail to start or exhibit visible jitter. A discrete-transistor Franklin oscillator, such as the one comprising Q_3 and Q_4 works better (**Figure 1**). This circuit also works well in the VCO (volt-

age-controlled-oscillator) portion of the synthesizer.

You use IC_{4A} , one-half of a 74HC390 dual decade-divider IC, to divide the 100-kHz reference into the 10-kHz frequency that the PLL uses. This 10-kHz square wave feeds one input of the phase comparator, IC_3 , and drives a voltage-tripler circuit comprising D_{12} through D_{15} . This tripler creates approximately 12V and obviates the need for a second higher-voltage power rail. You need the 12V to bias the VCO's varactor diode to the top of its tuning range.

The VCO, comprising Q_1 and Q_2 , runs at twice the desired output frequency. Varactor diode D_1 and inductor L_1 provide a tunable tank circuit. Any varactor for AM-radio tuning should

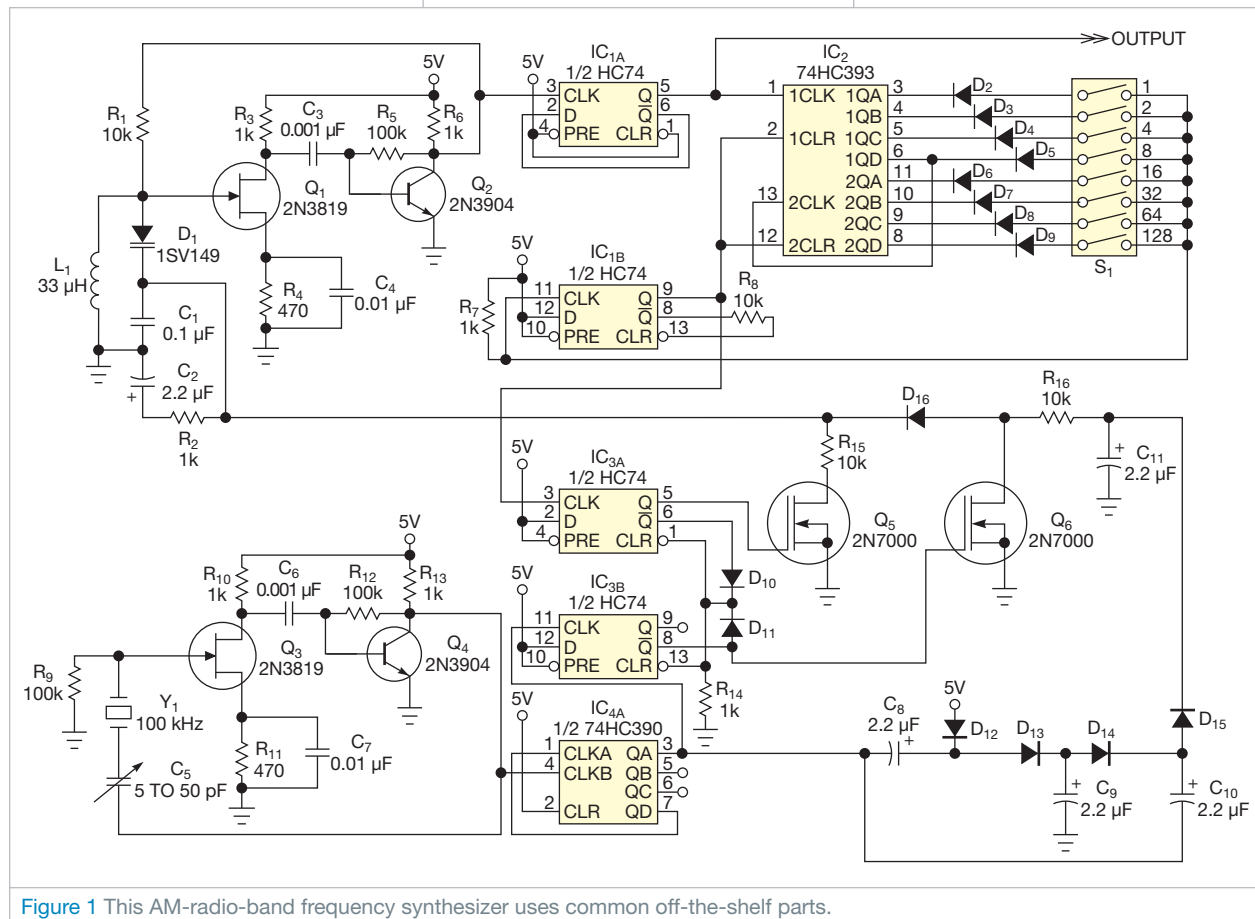


Figure 1 This AM-radio-band frequency synthesizer uses common off-the-shelf parts.

work. The capacitance of these diodes varies from 500 pF with no dc bias to 25 pF with a 12V reverse bias. IC_{1A} divides the LC oscillator by two to yield a symmetrical output waveform.

IC₂ further divides the VCO to the PLL's frequency. IC₂, an eight-stage binary counter, resets itself to zero when it reaches the desired count. IC_{1B}, a pulse-stretching one-shot, ensures that all sections of IC₂ reset at the target count. You program the divider with DIP switch S₁. Diodes D₃ through D₉ supply the necessary AND-logic function.


To set the synthesizer frequency, you first calculate the required divisor. For a 1140-kHz output, you must divide the VCO by 114 to equal the PLL's frequency of 10 kHz. You can close the DIP switches in S₁—in this case, switches 64, 32, 16, and 2—so that the numbers add up to the divisor: 114.

The PLL comparator is a three-state phase and frequency detector (Reference 1, in the online version of this Design Idea at www.edn.com/100624dib). When the divided VCO frequency is greater than 10 kHz, the \overline{Q} output of IC_{3B} goes high and

the Q output of IC_{3A} pulses at a 10-kHz rate. This action turns on Q₆, back-biasing D₁₆ to create a high-impedance state with respect to the 12V supply. Loop-filter capacitor C₂ then discharges through R₁₅ and Q₅. When the divided VCO is lower than the loop frequency, the Q output of IC_{3A} goes low, turning off Q₅ and creating a high-impedance state with respect to ground. Q₆ now pulses on and off, allowing C₂ to charge through D₁₅ and R₁₆. At PLL lock, Q₅ is off and Q₆ is on, except for a narrow “keep-alive” pulse at the loop frequency. **EDN**

Tricolor LEDs create a flashing array

Jeff Tregre, www.BuildingUltimateModels.com, Dallas, TX

 You can build a matrix of RGB (red/green/blue) LEDs using a simple and inexpensive circuit comprising the control logic and driver circuit in **Figure 1** and some LEDs (**Figure 2**). The cen-

ter RGB LED is the first to come on, after which each sequential LED in the 8×8-LED matrix follows. This process gives the appearance that the display is alive and moving outward. This sequence repeats,

producing a rainbow effect of colors.

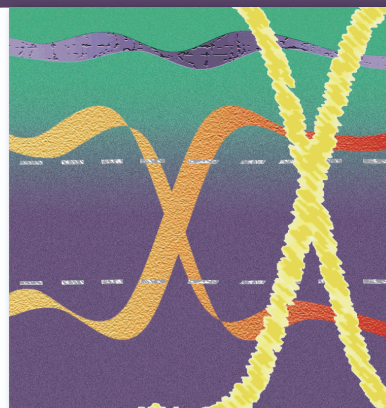
You can adjust the frequency of each clock by changing the values of R₁₇, R₁₉, and R₂₃. Use different frequencies for each clock, which will display eight colors from the 65 tricolored LEDs, because using the same frequencies for all the clocks causes your display to appear white. The cost of building this circuit

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should be \$25 to \$30. You can purchase 100 5-mm RGB LEDs from eBay for a total of about \$18. Be sure to use common-cathode LEDs.

This simple circuit comprises three clocks and three counters, one for each

of the three LED colors. Setting each clock frequency to a different rate causes each color of each LED to appear to be random. All resistors are 0.25W, except for R_3 , R_8 , and R_{13} , which are 0.5W; R_4 , R_9 , and R_{14} , which are 1W; and R_5 , R_{10} ,

and R_{15} , which are 1.5W resistors. These high-wattage resistors and the 12 NPN transistors are necessary because all LEDs in this matrix, except the center one, connect in parallel. Start by bending all of the ground leads flat and connecting

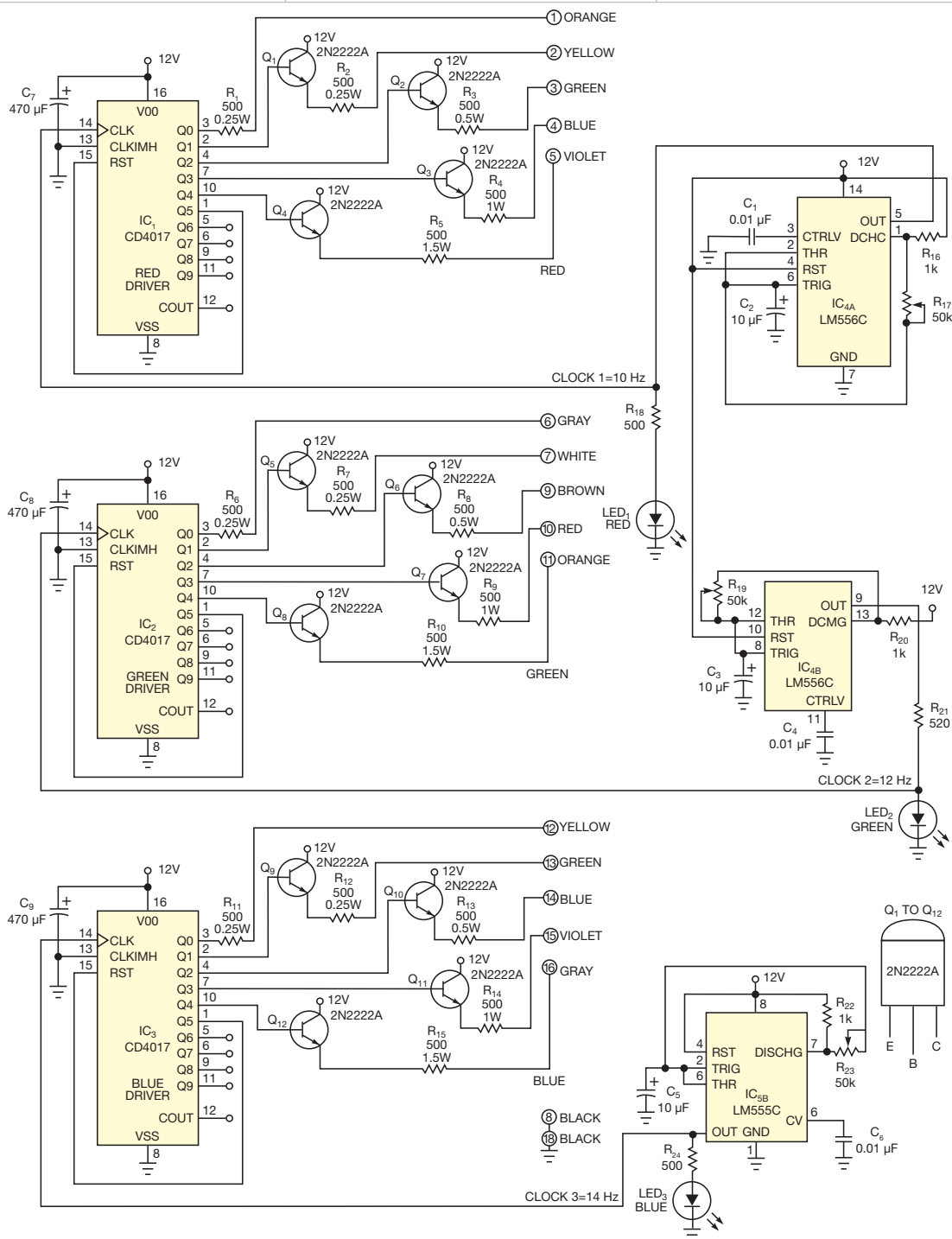


Figure 1 Three 555 timers generate clock signals, and CD4017 counters provide the drive signals for the transistors.

them together. When wiring the LEDs, begin in the center and work outward. You can then mount the LED board onto the top of the PCB (printed-circuit board). See the online version of this De-

sign Idea at www.edn.com/100624dic for photos, a parts list, and a video of this circuit in action.

To add the finishing touches to your project, use a small picture frame and in-

stall waxed paper onto the inside of the glass. Mount the LED board $\frac{1}{4}$ to 1 in. away. The magnifying lens of the LEDs will produce a beautiful effect when they shine through the waxed paper. **EDN**

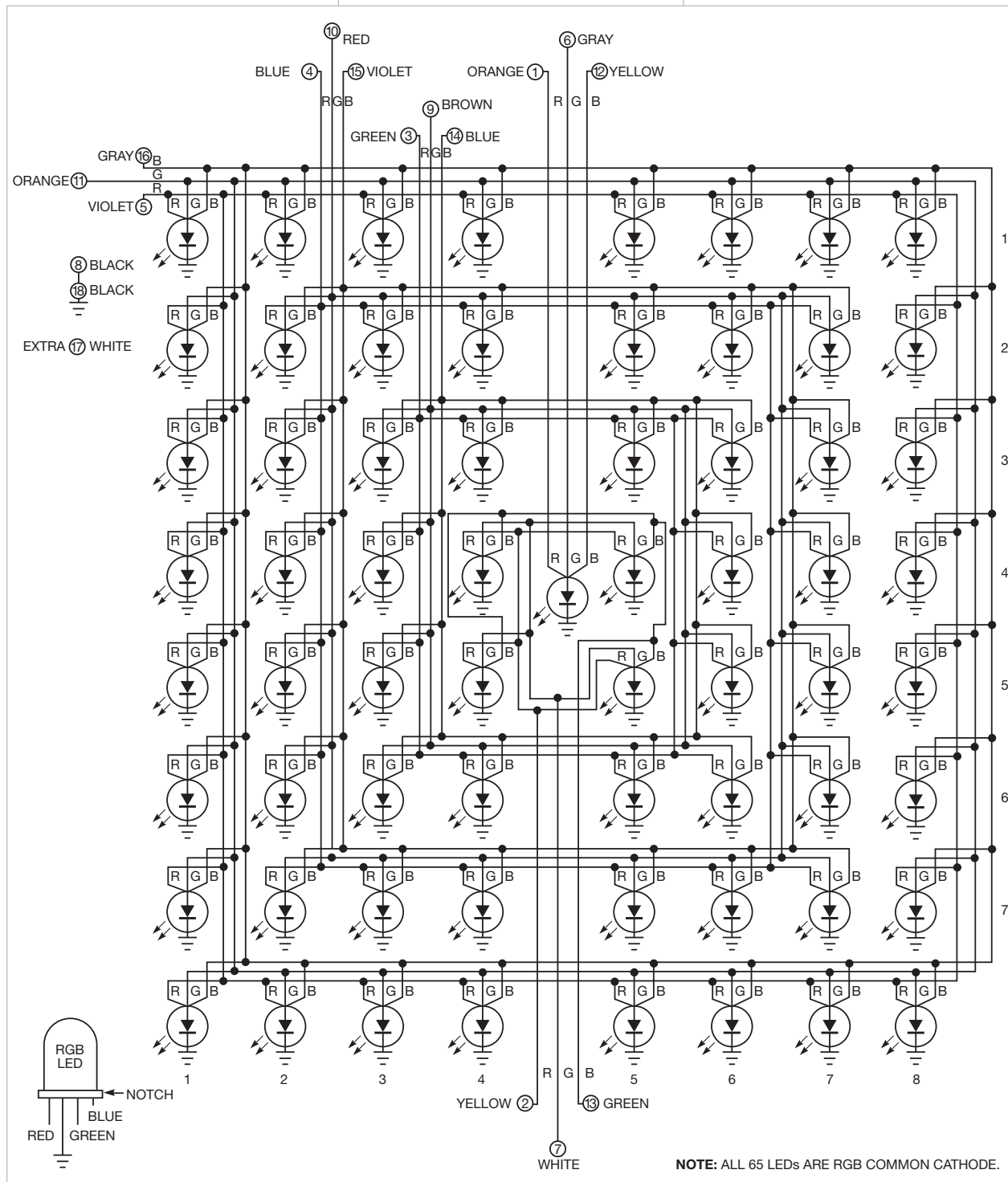
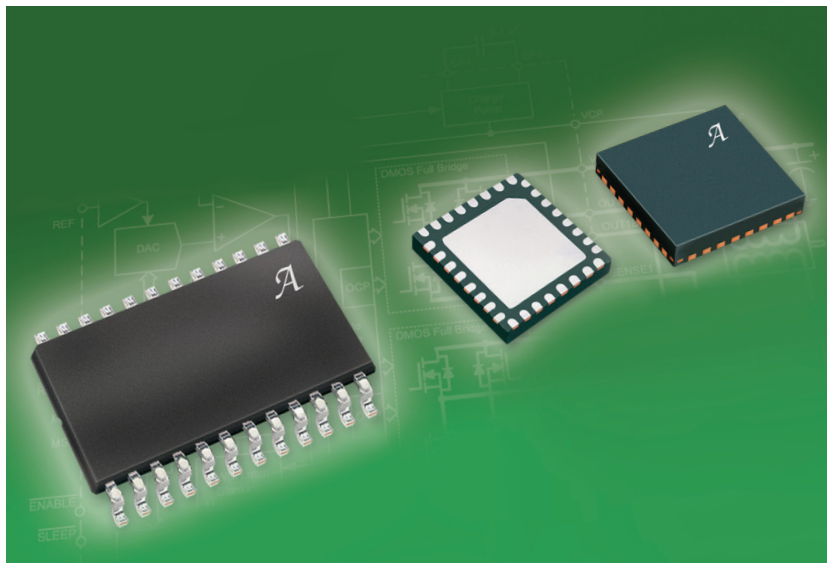


Figure 2 The LED in the center lights first, and the light then moves outward until the circuit produces an 8x8-LED display.

productroundup

MOTION



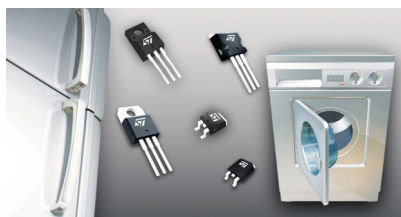
DMOS microstepping motor drivers feature overcurrent protection

➔ The A4982, A4984, A4985, and A4988 series of DMOS microstepping motor drivers include built-in translators for easy operation and overcurrent protection to reduce the rework cost in both manufacturing and normal operations. Targeting office automation, the devices operate bipolar stepper motors in full-, half-, quarter-, eighth-, and 16th-step modes, with an output-drive capacity as high as 35V and ± 2 A. They include fixed off-time current regulators, which can operate in slow or mixed decay modes. The translators allow the devices to drive the motor one microstep by inputting one pulse on the step input. The devices require no phase-sequence tables, high-frequency control lines, or complex interfaces to program. They come in several package options, including a 28- and 32-contact, 5 \times 5 \times 0.9-mm QFN. Prices range from \$1.21 to \$1.40, and prices for the 2A versions range from \$1.46 to \$1.68 (1000).

Allegro Microsystems, www.allegromicro.com

AC-motor switches cut cost of control for appliance applications

➔ The ACST4, ACST6, and ACST8 ac-motor switches tar-



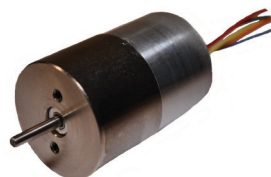
get use in appliance-control motors. The switches include a power triac that delivers enhanced commutation performance to turn off the motor without requiring external components to suppress voltage transients and to ensure reliable switching. Unlike conventional triacs, the switches also integrate protection against surge voltages as high as 2 kV on the ac line in accordance with the international IEC 61000-4-5. The ACST410 and ACST610 switches have a trigger current of 10 mA, allowing direct control by a CMOS device,

such as a microcontroller, without requiring a buffer or a driver. The ACST435 and ACST830 devices have noise immunity of at least 1000 and 2000V/ μ sec, respectively, complying with the IEC 61000-4-4 fast-transient-burst test and eliminating any need for conditioning of the trigger signal. The ACST4, ACST6, and ACST8 have 4, 6, and 8A maximum on-state current, respectively, and 800V blocking voltage. The family comprises 14 parts, and prices start at 70 cents (10,000).

STMicroelectronics, www.st.com

Linear-actuator family integrates position sensor in small package

➔ The LAS13 series of linear voice-coil actuators offers 6 mm of total stroke and 15.5N peak force in packages measuring only 1.3 in. in diameter and 1.1 to 1.8 in. long. The fully housed LAS13-18-000A incorporates an analog position sensor and self-alignment capabilities through its internal shaft bearings and is ready for drop-in installation. The model has a position accuracy of 10 to 20 microns.



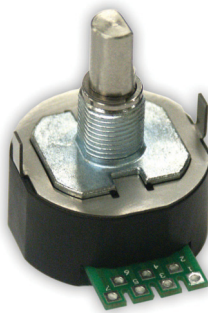
The fully housed LAH13-18-000A has the same self-alignment capabilities but without the position sensor. The semi-housed LA13-11-001A features self-alignment only, and the basic LA13-11-000A model has no housing, sensor, or alignment, so that customers can adapt it to their needs. The price for the fully integrated LAS13-18-000A is in the \$300s (production quantities).

BEI Kimco Magnetics,
www.beikimco.com

Noncontacting, 360° rotary position sensor features switch function and high-temperature operation



The programmable, noncontacting PSC-360 Hall-effect magnetic sensor features a switch function that lets you program the switching point at any angle, allowing maximum design flexibility. You can also use the device in multiturn applications. The device incorporates both on and off positions that provide a secondary position verification for improved safety, which is important for mission-critical applications in harsh environments.



The sensor operates at -40 to +150°C and has accuracy of 0.5% at 360°. The bushing/panel-mount-style sensor features a standard 1/4-in. D flat shaft in a

low-profile package measuring 13 mm. The sensor incorporates technology that is sensitive only to the flux density coplanar with the IC's surface, optimizing accuracy for absolute position feedback from 0 to 360°. The package maintains a true noncontacting air gap between the rotating magnet and the fixed sensing system. The device has a mechanical life of as many as 50 million cycles. The PSC-360 sells for less than \$20 (production quantities).

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www.piher.net

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Go on green



Troubleshooting a design—and adding things to that design to help in troubleshooting—is among the things engineers learn along the way. I learned this lesson during my first gig as a consultant. A crusty, old senior engineer had directed me to create a fixture, so I drew a schematic and gave it to the technician to build. When she was finished, she handed it to me. I tested and then disconnected it and put it on the senior engineer's desk.

About an hour later, he came stomping over to my desk and growled at me: “It doesn’t work; fix it.” I didn’t argue but went into the lab to see what the problem was. The power came in through a connector that was supposed to be impossible to connect backward. Nevertheless, the senior engineer had managed to put it in backward. Putting the connector in backward was easier than I had imagined and could become a trap for a new user. I correctly plugged in the connector and tried the circuit to see whether any damage from voltage reversal had occurred.

When I was satisfied that the board was undamaged, I started to think about how I could prevent this scenario or at least show that it had happened. I got

two LEDs—one red and one green—and two resistors out of the stockroom. I added these parts to the board so that, if a user correctly connected the power, the green LED would light. If the user incorrectly connected the power—that is, connected it backward—the red LED would light.

I reconnected the board to the test rig and informed the senior engineer that I had fixed it. He barked an acknowledgment, so I went off to do other things.

Until recently, every board I have designed has had at least one green LED to be able to start debugging when things go wrong. This arrangement lets me know that at least the power is connected and on. In other places, I add more LEDs to signal that things are

working—or not. I add probe points so that I can easily stick a meter or a scope probe onto the board to more quickly get to the bottom of the problem. I also add a place I can solder in a bare wire; I can clip a ground lead to this wire.

Recently, though, when designing a board for a client, I decided to omit the LED. It was a simple enough board, so what could go wrong?

Several days after my client received the board, I received a panicked e-mail. This message set off a frantic series of messages back and forth about the board’s not working to specification and signals’ feeding through to other signals. What was the problem? After a day of worry, the client realized, and sheepishly admitted, that he had correctly connected the power but had neglected to turn on the bench supply. Everything appeared to be working because the microcontroller got its power from the USB (Universal Serial Bus) line and the microcontroller LED was on. He didn’t make the connection that the power supply was off for more than a day. When he finally flipped on the power supply, everything was fine.

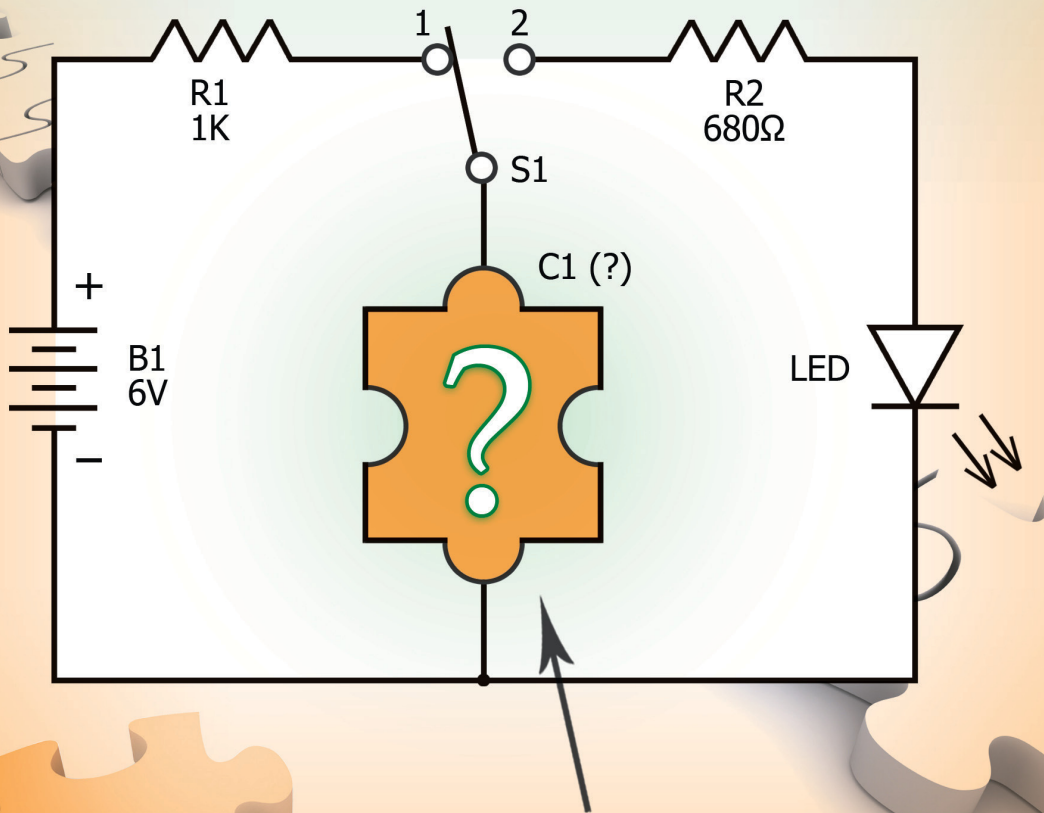
In the next revision, this board will get a green LED, too. Now, I take this step not just for me but also for my clients.

Here’s a recent update: A later version of this board added fuses and TVS (transient-voltage-suppressor) devices for ESD (electrostatic-discharge) protection. In addition, the client told me that the board was to be compatible with automotive power systems. From research, I found that automotive voltages can range from 7.2 to 28.8V. So I tested the board over that range and noted that, just below 10V, the LEDs flickered and went out. Debugging showed that the fuses had blown, but not why. I replaced the fuses and tried again, with the same result. It turned out that the chosen TVS had a clamp voltage of 9.6V. When the input got to that voltage, the TVS acted as a short circuit and blew the fuse, saving the board but screwing up my testing. **EDN**

Brian Conley is an engineer with Circuitsville Engineering LLC (Beaverton, OR).

www.edn.com/tales

Can You Solve This?



What is the missing component?



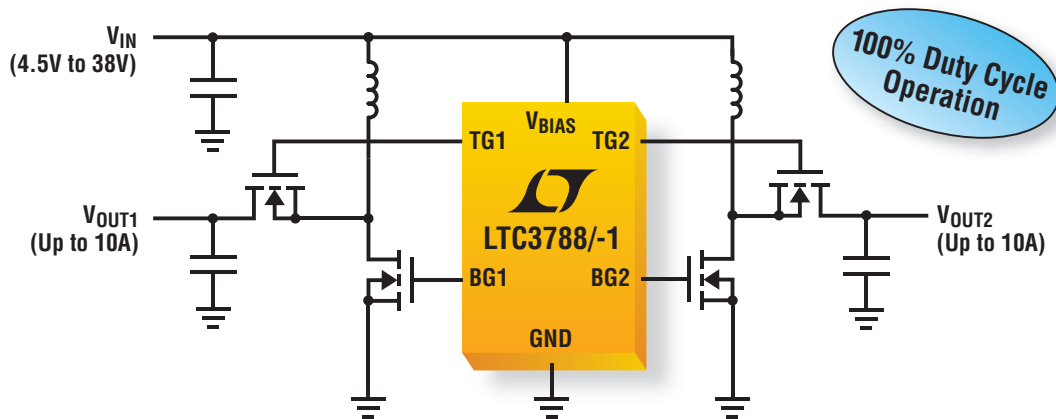
Electronics instructor Ollie Circuits planned to show his class of freshman electrical engineering students how to use a super capacitor as a memory back-up capacitor, but first he wanted to show how the students could make their own super capacitor and demonstrate its charge/discharge cycles with the simple circuit above. Most of the components were already on his workbench, the homemade super capacitor would be made from several layers of lemon juice-soaked paper towels interleaved between several layers of a mystery material to form a multi-layer stack. The stacked layers would then be sandwiched between the two copper-clad PC boards and held together with a rubber band. Ollie rushed to a nearby pet shop. What did he buy? Go to www.jameco.com/brain7 to see if you are correct and while you are there, sign-up for our free full-color catalog.

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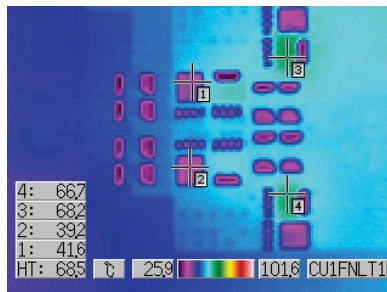


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